GaAs Nanowires: From Manipulation of Defect Formation to Controllable Electronic Transport Properties

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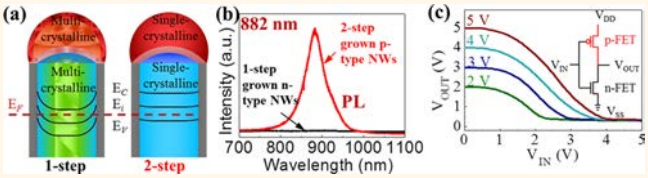
ABSTRACT Reliable control in the crystal quality of synthesized III−V nanowires (NWs) is particularly important to manipulate their corresponding electronic transport properties for technological applications. In this report, a "two-step" growth process is adopted to achieve single-crystalline GaAs NWs, where an initial high-temperature nucleation process is employed to ensure the formation of high Ga supersaturated Au_7Ga_3 and Au_2Ga alloy seeds, instead of the low Ga supersaturated Au_7Ga_2 seeds observed in the conventional "single-step" growth. These two-step NWs are long (>60 μm) and thick (>80 nm) with the minimal defect concentrations and uniform growth orientations. Importantly, these NWs exhibit p-type conductivity as compared to the single-step grown n-type NWs for the same diameter range. This NW conductivity difference (p- *versus* n-channel) is shown to originate from the donor-like crystal defects, such as As precipitates, induced by the low Ga supersaturated multi-crystalline Au_7Ga_2 alloy seeds. Then the well-controlled crystal quality for desired electronic properties is further explored in the application of large-scale p-type GaAs NW parallel array FETs as well as the integration of both p- and n-type GaAs NWs into CMOS inverters. All these illustrate the successful control of NW crystal defects and corresponding electronic transport properties *via* the manipulation of Ga supersaturation in the catalytic alloy tips with different preparation methods. The understanding of this relationship between NW crystal quality and electronic transport properties is critical and preferential to the future development of nanoelectronic materials, circuit design, and fabrication.



KEYWORDS: GaAs nanowires · two-step growth · crystal quality · defect formation · electronic transport · CMOS inverters

Recently, high carrier mobility III−V nanowire (NW) materials such as InAs, GaAs, InP, and GaSb have been extensively explored for alternative device channel materials because of the endless scaling of current silicon technology. In particular, the successful synthesis of InAs NWs with over ten thousands of electron mobility and InGaSb NWs with over several hundreds of hole mobility has yielded the promise of the development of next-generation high-performance electronics.[1−5] Nevertheless, there are still significant challenges to reliably control the crystal quality of synthesized NWs in order to manipulate the corresponding electronic transport properties. For example, crystal phase impurities, such as inversion domains between wurtzite and zinc blende structures, were demonstrated as electron trapping sites in both InAs and InP NWs, which can significantly vary the NW resistivity.[6,7] It is believed that these phase defects can modulate the local band structure of NWs, disturbing the carrier transport and modifying the NW conductivity.[6−8] On the other hand, although similar phase impurities had been observed for several studies in GaAs NWs,[9−11] another important III−V material system in electronics, photovoltaics, *etc.*, few report addressed the relationship between their crystal quality and electrical properties, in which these findings and the corresponding control are crucial since uncontrolled formation of these crystal defects would lead to unacceptable NW device characteristics and variability.

In our previous study, instead of controlling the crystal defects, utilizing the acceptor-like surface/interface states located between the intrinsic NW and its amorphous native

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oxide shell, p- to n-channel switching behaviors are observed for GaAs NW field-effect transistors (FETs), depending on the NW diameter. This oxide interface is shown to induce a space-charge layer penetrating deep into the thin nanowire to deplete all electrons, leading to inversion and thus giving p-type conduction in thin NWs as compared to the thick and intrinsically n-type NWs.[12] Following that, the growth mechanism of GaAs NWs was further investigated, illustrating that the small diameter NWs are single-crystalline and grown by low-melting-point high Ga supersaturated AuGa, Au_2Ga, and Au_7Ga_3 catalytic alloy tips, while the thick NWs obtained are highly defective and are grown by high-melting-point low Ga supersaturated Au_7Ga_2 multicrystalline tips.[13] In any case, the thick NWs with excellent crystal quality are highly essential for the implementation of various technological applications,[14−16] and all of these demonstrate the importance of well-controlled supersaturation of Au−Ga catalytic tips to achieve thick and single-crystalline GaAs NWs as well as potentially tailor the NW electronic properties.

In this regard, a "two-step" growth process is adopted here for the growth of single-crystalline and thick GaAs NWs,[17,18] where an initial high-temperature nucleation (alloying) process is employed to ensure the formation of high Ga supersaturated Au−Ga alloy, instead of the low Ga supersaturated alloys observed in the conventional "single-step" growth process. This way, the obtained NWs are long and thick with minimal defect concentrations and uniform growth orientations. When configured into NWFETs, these two-step grown NWs exhibit p-type conductivity as compared with the single-step grown n-type NWs for the same diameter range (>70 nm). These p-type characteristics are then further confirmed by the fabrication of parallel array NW devices *via* the contact printing[19] as well as by the integration with n-type NWs into CMOS inverters. This NW conductivity difference (p- *versus* n-channel) is shown to originate from the donor-like crystal defects, such as Ga vacancy and/or As precipitates induced by the low Ga supersaturated multicrystalline alloy seeds, to yield n-type behaviors in single-step grown GaAs NWs. As a result, the defect formation can be successfully manipulated by this enhanced two-step synthesis technique through the control of catalytic alloy supersaturation while the effect of crystal defects on corresponding NW electronic transport properties is further elucidated to provide the design guideline for achieving the optimal NW device performances.

RESULTS AND DISCUSSION

The GaAs NWs are grown by a solid-source chemical vapor deposition (SSCVD) method as reported before.[12,13,20] Briefly, in the single-step growth, the Au catalyst film predeposited on SiO_2/Si substrate

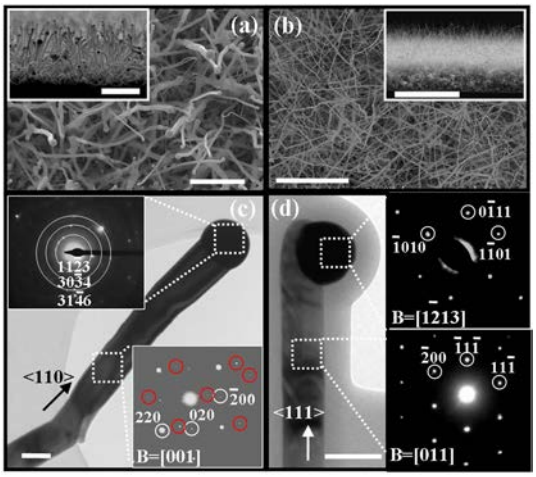

Figure 1. Comparison of the single- and two-step grown GaAs NWs. (a,b) SEM images of the single- and two-step grown NWs (scale bars are 2 and 10 μm, respectively). Insets show the corresponding cross-sectional SEM images illustrating the length of the NWs (scale bars are 10 and 50 μm, respectively). (c,d) TEM and SAED images of the single- and two-step grown NWs (scale bars are 100 nm). It is clear from the SEM images that the two-step grown NWs are longer and more uniform in diameter, with single crystallinity (low defect concentration) in both the NW body and Au_7Ga_3 alloy catalytic tips as compared with the single-step grown NWs.

pieces (with 50 nm thick thermal oxide) is placed in a downstream zone of a two-zone furnace, annealed at 800 °C and 10 min for the formation of Au nanoparticles, and then cooled to 600 °C for the GaAs NW growth. When the substrate is stable at 600 °C, the GaAs source powders in the upstream zone are heated to 900 °C and the evaporated precursors are transported to the nanoparticle catalysts by a H_2 flow (100 sccm). The only difference in the two-step growth is the addition of a nucleation step at 650 °C once the catalysts are annealed. After the catalysts are supersaturated at this temperature for 1 min, the substrate cools further to the growth temperature of 600 °C. The growth condition and duration (60 min) are then maintained the same for these two growth modes, and eventually, the system is cooled to room temperature for the NW harvesting and characterization.

Figure 1 compares the morphology and crystal quality of GaAs NWs grown by these single- and two-step processes utilizing the 12 nm thick Au film as the catalyst. It is clear that the single-step grown NWs are relatively short (~3 μm, as shown in Figure 1a inset); the NW diameter is varied substantially, while the two-step grown NWs are very long (~60 μm, as depicted in Figure 1b inset), and the diameter is rather uniform as observed from the scanning electron microscope (SEM) images. Even though all of these NWs consist of the same zinc blende crystal structure (Supporting Information Figure S1), the single-step grown NWs are highly defective as typically illustrated in the transmission electron microscope (TEM) image (Figure 1c) and the corresponding selected area electron diffraction

(SAED) pattern, whereas the two-step grown NWs exhibit single crystallinity without any significant defect concentrations (Figure 1d). All of these results indicate the advantages of the two-step growth method in the preparation of high-quality GaAs and ternary InGaAs NWs.[21,22] It is noted that, although a similar pioneer work was reported for the synthesis of GaAs NWs epitaxially on GaAs(111)B substrate in a metal–organic (MO) CVD system,[17] the proposed mechanisms might not applicable to our results. Specifically, our GaAs NWs are grown on noncrystalline SiO_2/Si substrates in a SSCVD system; therefore, the proposed improvement in the Au/GaAs substrate/interface registry does not exist in this current two-step growth technique. Moreover, since the Au–Ga catalysts (with 10 atom % Ga concentration) are confirmed to exist in the solid phase even at our growth temperature of 600 °C by electron diffraction,[23,24] another proposed melting/solidification hysteresis of the Au–Ga alloy formation might not take place here. As a result, the underlying physical mechanism of this two-step process is then further explored to illustrate its growth characteristics for the achievement of crystalline and thick GaAs NWs.

From the widely accepted vapor–liquid–solid (VLS) and/or vapor–solid–solid (VSS) growth mechanisms, Ga diffuses from the Au–Ga catalyst and precipitates to react with the As_2 precursor to form the GaAs NWs in which the supersaturation of the Au–Ga alloy would play a significant role in governing the physical properties of grown NWs.[25,26] In addition, we have demonstrated in our previous study that the crystal phase and orientation of Ni-catalyzed GaAs NWs are highly dependent on the crystal structure of the Ni–Ga alloy catalyst.[27] Consequently, the Au–Ga catalyst alloys that exist in these single- and two-step growth processes are investigated in detail in order to assess the difference in the corresponding NW formation. From SAED patterns of the Au–Ga catalysts illustrated in the insets of Figure 1c,d, it is obvious that the Au–Ga tip is present as the multicrystalline Au_7Ga_2 alloy in the single-step growth, while it exhibits the single-crystalline Au_7Ga_3 phase in the two-step growth. To further evaluate the multicrystalline details of the Au_7Ga_2 alloy (single-step growth), cross-sectional high-resolution (HR) TEM images are taken as shown in Supporting Information Figure S2, where the alloy tip is determined to consist of a thin (~10 nm) Au_7Ga_3 shell (undetectable by SAED) and a thick (>150 nm) Au_7Ga_2 core. Notably, both the shell and the core reveal multicrystallinity as indicated by the fast Fourier transformation (FFT). Moreover, the single-crystalline Au_2Ga alloy catalytic tip is also found in the two-step growth (Supporting Information Figure S3), inferring the formation and its role of high Ga supersaturated Au–Ga alloy tips for the realization of GaAs NWs with excellent crystal quality in this work.

It is believed that the low Ga supersaturated Au_7Ga_2 alloy (~22.2 atom % Ga) might not be sufficiently activated in the single-step growth due to its relatively higher melting point (~500 °C) from the binary phase diagram;[24] as a result, the multicrystalline Au–Ga alloy would be obtained and thus induce an inhomogeneous and insufficient Ga precursor diffusion, leading to the defective GaAs NW formation. In contrast, the high Ga supersaturated Au_7Ga_3 (30 atom % Ga, melting point ~348.8 °C) and Au_2Ga (33.3 atom % Ga, melting point ~339.4 °C) alloys can be easily activated, and the resulting single-crystalline structure yields a faster Ga diffusion, inducing a faster NW growth rate as well as better crystal quality. In our previous study, Au_7Ga_2 alloy tips were always found for NWs with a diameter >40 nm in the single-step growth, giving defective n-type GaAs NWs.[12] In the two-step method, due to the supplemented alloying process (additional nucleation step at 650 °C), the degree of Ga supersaturation in the Au–Ga tips can be further enhanced even for NWs with a diameter up to 150 nm, leading to the realization of thick and defect-free GaAs NWs. Although intuitively from the Gibbs–Thomson equation, $\ln(C_d/C_0) = 4\gamma V_m/(dRT)$, where C_d is the concentration of Ga in the Au nanoparticle with diameter of d, C_0 is the equilibrium concentration on a flat surface ($d \rightarrow \infty$) materials, γ is surface energy (1.39 J m^{-2} in liquid), V_m is molar volume of Au (11.38 cm^3 mol^{-1}, in molten phase), R is constant (8.314 J mol^{-1} K^{-1}), and T is the growth temperature,[28,29] the Ga supersaturation is reversely proportional to the temperature, one should also notice that the high-temperature single-crystalline phase would have a higher V_m and a higher γ;[29,30] therefore, it would eventually result in a slightly higher Ga supersaturation, such as forming the high Ga supersaturated Au_7Ga_3 and Au_2Ga alloy tips in the two-step growth, as compared to the low Ga supersaturated multicrystalline phase of the Au_7Ga_2 alloy, as detailed in the Supporting Information.

To shed light to further compare the growth differences, the NW growth rate, density, diameter variation, as well as the orientation distribution are all summarized in Figure 2, with nominal Au thin film thicknesses of 0.5, 2.5, 4, 6, and 12 nm. It is clear from Figure 2a that the growth rate of the two-step grown NWs is much faster than that of the single-step grown NWs, as a result of the faster diffusion velocity of Ga precursor through the higher Ga supersaturated Au–Ga alloy. Likewise, the growth rate is also faster for small diameter NWs than their thicker counterparts due to the higher Ga supersaturation in small diameter nanoparticles as inferred from the Gibbs–Thomson effect.[13] Notably, the NW growth density is similar between these two growth processes in all Au film thicknesses. However, the NW diameter distribution (statistics of more than 100 NWs from TEM images) is much tighter for the two-step grown NWs as depicted in the mean

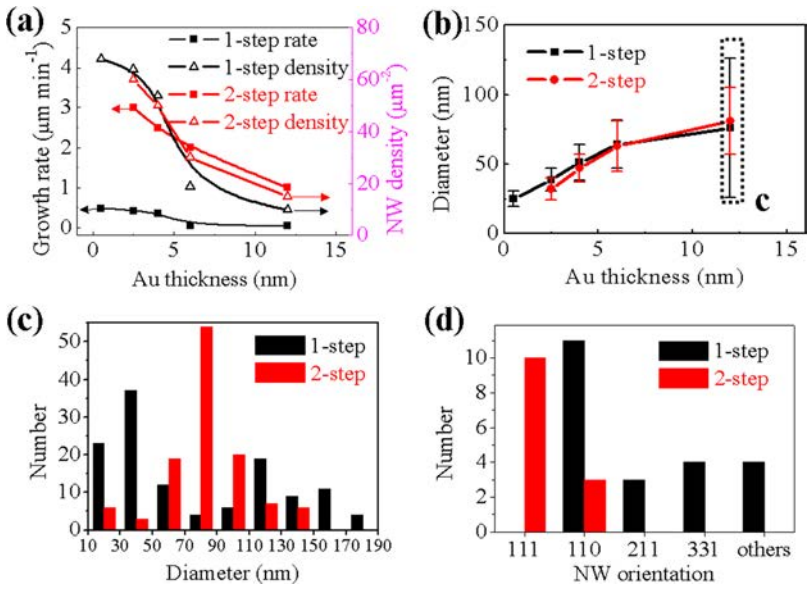

Figure 2. Comparison of the NW growth rate, density, diameter distribution, and orientation statistics between the single- and two-step grown GaAs NWs. (a) Growth rate, density, and (b) NW diameter as a function of different nominally thick Au catalyst film, (c) diameter distribution of GaAs NWs grown by the 12 nm thick Au catalyst, and (d) NW growth orientation statistic. It is clear that the two-step grown GaAs NWs have faster growth rate, similar density, tighter diameter distribution, and more uniform crystal orientations as compared with the ones obtained in the single-step method.

diameter and standard deviation in Figure 2b. For example, the diameter histogram of the NWs grown by a 12 nm thick Au catalyst is shown in Figure 2c, where one can clearly see two peaks (30−50 and 110−130 nm) for single-step grown NWs while a more uniform and more Gaussian shaped diameter distribution is evidently observed for the two-step growth. In the single-step process, the NW growth is initiated before the Au catalyst film is fully activated by the Ga precursor, and thus higher Ga supersaturated small particles would lead to long and thin NWs as reported before,[13] leaving the other lower Ga supersaturated large particles for the short and thick NW growth. On the contrary, during the high-temperature nucleation step, the Au particles are more uniformly and highly Ga supersaturated and the surface atoms are more mobile so that all of these would lead to the narrower diameter distribution and faster growth rate of NWs in the two-step growth. More importantly, this two-step method can yield GaAs NWs with uniform growth orientation, dominantly in the ⟨111⟩ and ⟨110⟩ directions (Figure 2d and Supporting Information Figure S4), as compared with a mixture of orientations in ⟨110⟩, ⟨211⟩, ⟨331⟩, *etc.* for the single-step growth. The preferred ⟨111⟩ growth orientation might also originate from the fast Ga diffusion from the higher Ga supersaturated Au−Ga alloys (*i.e.*, Au_7Ga_3 and Au_2Ga) because the (111) planes have the largest atomic density to consume the fast diffused Ga precursor atoms, similar to the phenomenon observed in thin NWs (diameter <40 nm) where ⟨111⟩-oriented NWs are produced due to the fast Ga diffusion in the high Ga supersaturated Au−Ga alloys.[13]

On the other hand, as opposed to the previously reported single-step growth that gives thick (diameter >70 nm) n-type NWs,[12] the GaAs NWs grown by the two-step method (diameter ∼10−150 nm) all exhibit p-type characteristics as illustrated in the $I_{DS}-V_{GS}$ curves after fabricated back-gated NW field-effect transistors (FETs) (Figure 3a,b). At the same time, since the thick NWs can be grown much longer *via* this two-step technique (Figure 1b), it can enable the efficient NW contact printing[19,21] to fabricate parallel array NWFETs (Figure 3c,d) for potential large-scale device applications. Based on the SEM images, the printed density is ∼1 NW/μm accounting for a total number of ∼50 NWs in the 50 μm wide channel (NW diameter ∼80 nm), in which the parallel array ON current is roughly 50 time the one in the single NW device. This way, the parallel array NWFET further verifies the p-channel conduction, which is confirmed to rule out the n-type possibility by wire-to-wire variation. In fact, this p-type conducting mechanism has been studied previously for the single-step technique where the surface oxide layer consists of a lot of trap states depleting free electrons in the GaAs NWs.[12] Quantitatively, this depletion layer can be estimated as 10−30 nm by the equation $W = (2\varepsilon\varphi/eN)^{1/2}$, where W is depletion layer thickness, ε is the dielectric constant of GaAs (∼13.1), φ is the surface barrier potential, e is the electronic charge, and N is the carrier density. As a result, this surface effect plays a more dominant role in the thin NWs (diameter <40 nm), which accounts for the carrier inversion exhibiting the p-type behavior, while crystal defects in the thick NWs (diameter >70 nm) contribute free electrons, leading to the

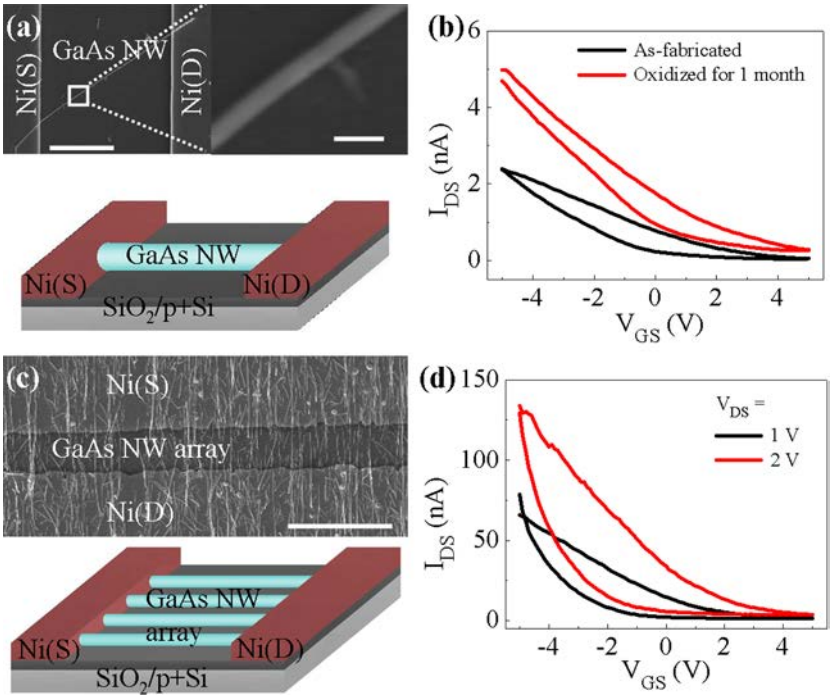

Figure 3. Typical electrical characteristics of the two-step grown thick GaAs NWs when configured into FETs. (a) SEM image and device schematic of the single NWFET (scale bars are 5 μm and 200 nm, respectively). (b) Corresponding $I_{DS}-V_{GS}$ curves (V_{DS} = 1 V) of the as-fabricated FET and the one oxidized in ambient for 1 month. (c) SEM image and device schematic of parallel array NWFET (scale bar = 10 μm). (d) Corresponding $I_{DS}-V_{GS}$ curves of the FET.

n-type conductance. In this case, the aforementioned mechanism is also expected to be applicable to this two-step grown p-type thick NWs, because far less crystal defects result here which donate less free electrons. This minimal electron concentration can then be fully depleted by the surface oxide layer yielding the p-type characteristics. As presented in Figure 3b, this assumption is further verified by the fact that the ON current increases after the NW channel has been oxidized in ambient for 1 month, with the thicker surface depletion layer contributing to the higher p-type current.

In order to further verify the above-mentioned crystal quality difference between these two growth techniques, accounting for the different electrical behaviors, room temperature photoluminescence (PL) (632.8 nm laser excitation) was performed on these 80 nm thick GaAs NWs (Figure 4a). It is evident that the two-step grown NWs have a PL peak of ~882 nm (~1.41 eV), which is in good agreement with the band gap of bulk zinc blende GaAs material (~1.42 eV) as the blue-shifted PL is not usually observed for a NW diameter >20 nm.[28,31,32] More importantly, the single-step grown NWs do not display any luminescence before or after the $(NH_4)_2S$ passivation (data not shown). In this case, this quenched PL can be attributed to the presence of crystal defects, instead of the surface traps, acting as nonradiative recombination centers. In the meanwhile, these crystal defects are then further characterized by Raman spectroscopy (514 nm excitation). As depicted in Figure 4b, there are longitudinal optical (LO(Γ) ~ 289 cm^{-1}) and transverse optical (TO(Γ) ~ 268 cm^{-1}) phonons at Γ point, as well as LO phonons at the zone edge (LO ~ 248 cm^{-1}) in the spectra of both single-step and two-step grown GaAs NWs.[33,34] In detail, the LO peak is typically induced from the stress and disorders in the buffer layer between NWs and the SiO_2 substrate.[33,35,36] Also, the LO(Γ) peak width is observed to be broader, and the relative peak intensity of LO(Γ) with respect to TO(Γ) is significantly lower for the defective single-step grown NWs as compared with the two-step ones (Supporting Information Figure S5). It is noted that, although the Raman selection rule is different at varied surfaces, such as LO(Γ) is allowed at (100) and (111) planes while TO(Γ) is allowed at (110) and (111) planes,[37] the wider and lower relative peak intensity of LO(Γ) probably originates from the related crystal defects such as As precipitates in the randomly distributed GaAs NWs.[33,38−40] Considering the growth mechanism described, there would be deficient Ga precursor diffusion in the lower Ga supersaturated multicrytalline Au_7Ga_2 alloy tips in the single-step growth in contrast to the case of high Ga supersaturated Au_7Ga_3 and Au_2Ga tips, leading to the formation of point defects such as Ga vacancy (V_{Ga}), As antisite (As_{Ga}), or As precipitates. Notably, these As precipitates are found preferably segregated along the grain boundary and dislocation in these defective multicrystalline GaAs materials.[39] This way, these As-rich (Ga-deficient)

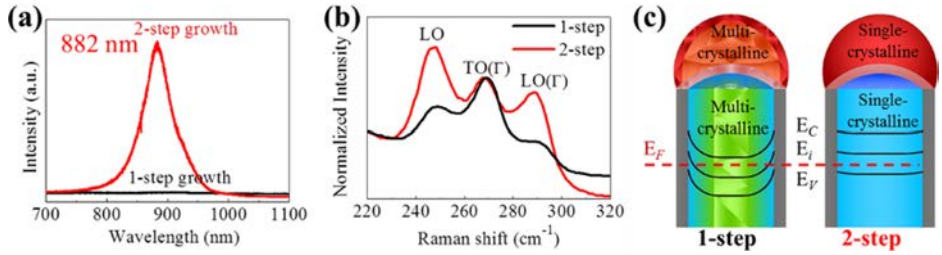

Figure 4. Crystal defect characterization between the single- and two-step grown GaAs NWs. (a) Room temperature PL spectra, showing a good crystal quality of the two-step grown NWs, lacking nonradiative recombination centers. (b) Raman spectra with a lower LO(Γ)/TO(Γ) peak intensity ratio indicating the existence of arsenic precipitates in the single-step grown NWs. (c) Cross-sectional view of NWs with the corresponding crystal quality and equilibrium energy band diagram at the zero gate bias. Specifically, the single-step grown NWs are highly defective as a result of the multicrystalline Au−Ga catalytic alloy. These defects contribute to numerous free electrons which cannot be depleted by the surface oxide layer contributing the n-type behavior. On the contrary, the two-step grown NWs have enhanced crystal quality, and a small number of the free electrons can be fully depleted by the surface oxide trap states, leading to the p-type conductance.

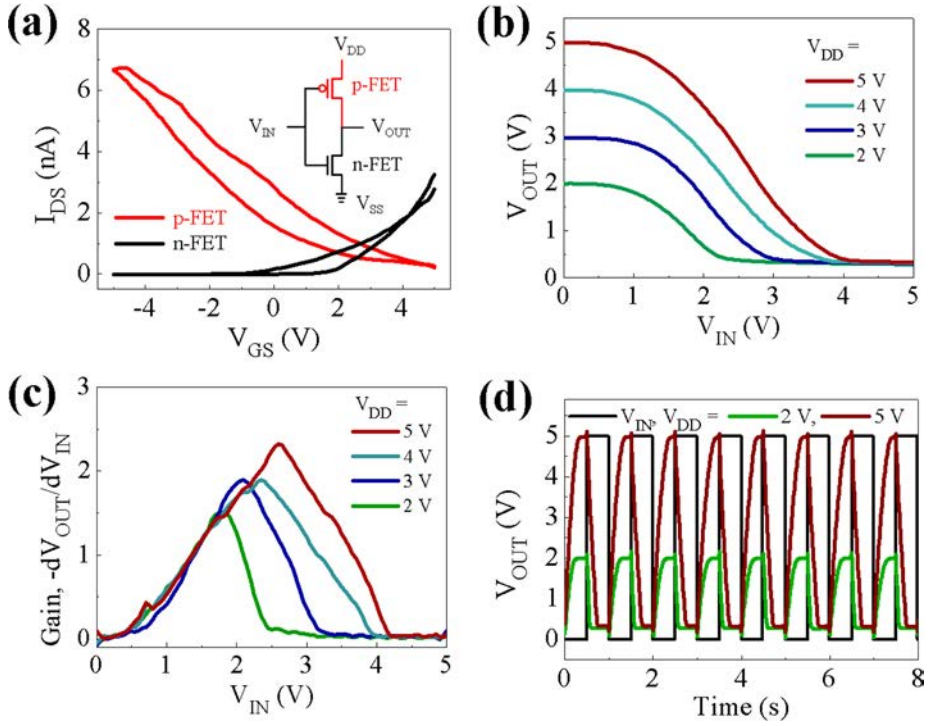

Figure 5. CMOS inverter composed of FETs with one p-type NW (two-step grown) and one n-type NW (single-step grown). (a) $I_{DS}-V_{GS}$ curves of the corresponding p-FET and n-FET, and the inset illustrates the circuit diagram. (b) Transformation curves of the typical NW CMOS inverter. (c) Corresponding gain as a function of input voltage. (d) Output response to alternating voltage input of 1 Hz.

crystal defects would behave as donor-like defects and contribute to the n-type characteristics in the single-step grown NWs as observed in the corresponding NWFETs. In an effort to visualize the effect of NW crystal quality in modulating the electronic transport properties, Figure 4c shows the cross-sectional schematics along the NWs between single- and two-step growth with the corresponding crystal quality and equilibrium energy band diagram at the zero gate bias. Specifically, as discussed above, the multicrystallinity and crystal defects (*e.g.*, As precipitates) that exist in the single-step grown NWs donate a lot of free electrons, which cannot be fully depleted by the surface oxide traps; thus the Fermi level stays near the conductance band, making the NWs n-type behavior. In the two-step growth, NWs consist of enhanced crystal quality such that less free electrons are present, which can be easily depleted by the surface trap layer for the p-type conductance.

At the end, the controllable formation of these p-type and n-type GaAs NWs obtained *via* different growth techniques through the manipulation of crystal defects is further verified and illustrated by the integration of these NWs into CMOS inverters,[1,4] as shown in Figure 5 with the device fabrication details shown in Supporting Information Figure S6. The typical $I_{DS}-V_{GS}$ curves of the p- and n-type NWFETs for the formation

of the inverter are depicted in Figure 5a, with the circuit diagram shown in the inset. Transformation curves of the fabricated inverter are presented in Figure 5b, where the output voltage is clearly transformed to the inverse of the input with different V_{DD} of 2−5 V (0 V is logic "low", while 2−5 V is logic "high"). A gain (defined as $-dV_{OUT}/dV_{IN}$) of ~2.5 is demonstrated (Figure 5c) with the response to alternating voltage at 1 Hz with V_{DD} = 2 and 5 V (Figure 5d). All of this confirms the validation of *in situ* transformation of the input voltage. Although there is still a margin for the inverter to enhance the gain to enable higher frequency response, such as utilizing the top-gate configuration and source/drain contact annealing,[41,42] it is the first illustration of an all intrinsic unintentionally doped GaAs NW fabricated CMOS inverter, showing the successful modulation of NW electronic transport properties by simply controlling the crystal quality, holding the promise for next-generation NW electronics by this facile manipulation in the catalytic alloy supersaturation.

CONCLUSIONS

In summary, GaAs NWs with the improved crystal quality, minimal defect concentration, as well as uniform growth orientation have been achieved utilizing a two-step growth method, in which an additional high-temperature nucleation step is introduced before the typical NW growth. This extra step is found to yield the high Ga supersaturation to achieve Au_7Ga_3 and Au_2Ga catalytic alloy tips and thus makes Ga diffusion more efficient from the tips to form high-quality NWs. Importantly, these two-step grown NWs exhibit p-type characteristics, which is attributed to the minimal free electron concentration arising from the significant reduction of donor-like crystal defects (*e.g.*, As precipitates). This way, these electrons can be easily depleted by the surface oxide trap states, leading to the p-type behavior, as compared to the n-type characteristics observed in the defective thick NWs obtained in the conventional single-step growth. Moreover, these p-type characteristics are further confirmed by the fabrication of parallel array NW devices as well as by the integration between both p- and n-type GaAs NWs into CMOS inverters. All of these results illustrate the successful control of NW crystal defects as well as electronic transport properties *via* the manipulation of Ga supersaturation in the catalytic alloy tips with different preparation methods. The understanding of this relationship between NW crystal quality and electronic transport properties is critical and preferential to the future development of nanoelectronic materials, circuit design, and fabrication.

METHODS

GaAs NW Growth. GaAs NWs used in this study were prepared in a dual-zone horizontal tube furnace as previously reported.[12,13,20] Briefly for single-step growth, the solid source (1 g, GaAs powder, 99.9999% purity, placed in a boron nitride crucible) was evaporated at the center of the upstream zone, while the growth substrate (various thickness of Au catalyst film predeposited on SiO_2/Si) was placed in the middle of the downstream zone with a tilt angle of ~20° and a distance of 10 cm away from the source. In order to tailor the diameter of Au particles for different catalytic composition and degree of Ga supersaturation, Au films with a nominal thickness of 0.5 to 25 nm were thermally evaporated under a vacuum of ~1×10^{-6} Torr onto the substrates. During the NW growth, the substrate was thermally annealed at 800 °C for 10 min in a hydrogen environment (99.999% pure H_2, 100 sccm, 1 Torr) to obtain Au nanoclusters with different sizes as the catalysts. When the substrate temperature was cooled to the preset growth temperature (590−610 °C), the source was heated to the required source temperature (900−925 °C) for a duration of 1 h. After the growth, the source and substrate heater were stopped together and cooled to room temperature under the flow of H_2 gas. An additional alloying process was adopted in the two-step growth at 640−660 °C right after the catalyst annealing and then cooled to the growth temperature of 590−610 °C, with the other operation kept the same as that of the single-step growth.

Characterization. Surface morphologies and growth length of the grown NWs were observed with SEM (FEI/Philips XL30) and TEM (Philips CM-20). Crystal structures were determined by imaging with a high-resolution TEM (JEOL 2100F) and studying with the SAED (Philips CM-20). For the TEM imaging, GaAs NWs were first suspended in the ethanol solution by ultrasonication and drop-casted onto the grid for the corresponding characterization. The micro-photoluminescence (μPL) spectra were measured by a 632.8 nm laser excitation at a power density of 1.7 W cm^{-2}, and the Raman spectra were gained by a 514 nm Ar^+ laser excitation.

FET Fabrication. GaAs NWFETs were fabricated by drop-casting the NW suspension onto highly doped p-type Si substrates with a 50 nm thermally grown gate oxide. Photolithography was utilized to define the source and drain regions with a 10 μm channel length using AZ5206E photoresist, and 80 nm thick Ni was thermally deposited as the contact electrodes followed by a lift-off process. Electrical performance of fabricated back-gated FETs was characterized with a standard electrical probe station and Agilent 4155C semiconductor analyzer.

The parallel array NWFETs were fabricated by the contact printing technique as reported before.[19,21] First, a channel pattern was defined by lithography on the SiO_2/Si substrate, which was then subjected to oxygen plasma (50 W, 10 s) to make the exposed SiO_2 surface hydrophobic. A polylysine (5% in water) solution was dropped onto the pattern to attach the functional groups on the SiO_2 surface for 10 min. The wafer was then blow dried by N_2 and placed on a horizontal plate, and the NW donator was then placed on top of it. After the NW donator was pushed through the acceptor pattern, NWs were anchored on the SiO_2 surface. The NW arrays were next washed with acetone to remove the residual photoresist, and the FET device was fabricated by conventional photolithography.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: XRD patterns; cross-sectional HRTEM of Au−Ga catalyst in single-step growth; SAED pattern of Au−Ga catalyst in two-step growth; supersaturation comparison in single- and two-step growth; growth orientation of GaAs NWs by two-step growth; Raman spectra comparison; and CMOS inverter images. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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