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High-Sensitivity Floating-Gate Phototransistors Based on WS_2 and MoS_2

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In recent years, 2D layered materials have been considered as promising photon absorption channel media for next-generation phototransistors due to their atomic thickness, easily tailored single-crystal van der Waals heterostructures, ultrafast optoelectronic characteristics, and broadband photon absorption. However, the photosensitivity obtained from such devices, even under a large bias voltage, is still unsatisfactory until now. In this paper, high-sensitivity phototransistors based on WS_2 and MoS_2 are proposed, designed, and fabricated with gold nanoparticles (AuNPs) embedded in the gate dielectric. These AuNPs, located between the tunneling and blocking dielectric, are found to enable efficient electron trapping in order to strongly suppress dark current. Ultralow dark current (10^{-11} A), high photoresponsivity (1090 A W^{-1}), and high detectivity (3.5×10^{11} Jones) are obtained for the WS_2 devices under a low source/drain and a zero gate voltage at a wavelength of 520 nm. These results demonstrate that the floating-gate memory structure is an effective configuration to achieve high-performance 2D electronic/optoelectronic devices.

1. Introduction

Over the past few years, 2D layered materials have attracted intensive interests for their unique electrical and optical properties.[1–10] For instance, graphene has been widely used as the active material for high carrier mobility and ultra-broadband phototransistors, optical modulators, plasmonic devices as well as ultrafast lasers.[4–8] In addition to graphene, tungsten disulfide (WS_2), built up of layered S-W-S atoms bonded by van der Waals forces, has also received renewed attention.[11–25] WS_2 is a typical semiconducting 2D material with a band gap ranging from 1.3 to 2.05 eV, depending on the number of stacking layers.[11,12] It exhibits unique properties including low effective mass, theoretical high carrier mobility of over 1000 $cm^2\ V^{-1}\ s^{-1}$,[13,14] high quantum efficiency, and thermal stability.[15,16] Field-effect transistors based on few-layer WS_2 possess a high ON/OFF current ratio of 4×10^6, an impressive drain current density of 380 $\mu A\ \mu m^{-1}$, and a peak field-effect mobility of 60 $cm^2\ V^{-1}\ s^{-1}$.[17] Because of these unique features, WS_2 has become a potential candidate material for future electronic and optoelectronic applications. However, photoresponsivity of the monolayer WS_2 synthesized by chemical vapor deposition (CVD) is reported to be only 18.8 mA W^{-1} in a vacuum even when applying a substantially high gate voltage (60 V) and a large drain bias (V_{ds} = 20 V).[26] These high voltages not only cause high energy consumption, but also lead to a significant increase in the leakage current of fabricated devices, which degrades the corresponding specific detectivity, D^*.[27,28] As for the mechanically exfoliated WS_2, fabricated phototransistors still demonstrate low responsivity ranging from 0.1 to 5.7 A W^{-1},[29–32] which is already three orders of magnitude higher than that of CVD due to the reduced trap densities. Nevertheless, the high operating voltages would still induce substantially high leakage current. To the best of our knowledge, the record photosensitivity of WS_2 phototransistors is 884 A W^{-1}, which is measured in a NH_3 atmosphere. In that case, NH_3 serves as electron donors to the WS_2 surface that results in high channel conductance, as well an increase in the dark current to 10^{-7} A.[29]

With the aim to mitigate this performance issue, a multilayer WS_2 phototransistor based on a floating-gate memory structure is proposed, designed, and fabricated with excellent optoelectronic properties. To suppress the dark current in the device channel, gold nanoparticles (AuNPs) placed between the tunneling and blocking dielectric layers are employed as a charge trapping layer.[33] In this way, electrons trapped in the AuNPs would deplete the intrinsic carrier concentration. More importantly, high detectivity (3.5×10^{11} Jones) and photoresponsivity (1090 A W^{-1}) can be now achieved under a low V_{ds} (20 mV) and

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a zero gate voltage in a vacuum (5×10^{-2} Pa) with an ultralow dark current (10^{-11} A). In order to further demonstrate the versatility of the proposed floating-gate memory structure, we also conFigure a floating-gate MoS_2 phototransistor with the respectable photoresponsivity of 59.2 A W^{-1}, and detectivity of up to 3.8×10^{10} Jones.

2. Results and Discussion

2.1. Device Structure and Electrical Characterization of the WS_2

Figure 1a shows the structural schematic of the fabricated device while Figure 1b displays the corresponding top-view scanning electron microscope (SEM) image. It is clear that multilayer WS_2 is mechanically exfoliated onto the thermally grown SiO_2 layer with a thickness of 255 nm, in which the thickness is identified by Raman spectra[34–36] and optical images (Figure S1, Supporting Information). Electron-beam lithography (EBL) is then used to define the source/drain patterns followed by the deposition of Cr/Au (15/50 nm) electrodes. After the lift-off process, a 6.5 nm thick HfO_2 tunneling oxide is deposited by atom layer deposition (ALD) at 95 °C. Due to the lack of sufficient dangling bonds on the surface of WS_2, 1 nm thick Al is deposited as the seeding layer before the ALD process in order to achieve a uniform and conformal tunneling oxide layer.[37] Next, the charge trapping layer of 1 nm thick AuNPs (as shown in the atomic force microscope (AFM) image in Figure S2, Supporting Information) is deposited by thermal deposition under a vacuum of 6×10^{-4} Pa. Following this step, 20 nm thick HfO_2 is formed deposited by ALD onto the entire surface as the blocking layer followed by the deposition of 100 nm thick indium tin oxide (ITO) achieved by magnetron sputtering at room temperature as the control gate. Finally, the device is thermally annealed at 200 °C for 2 h in high purity nitrogen in order to increase the conductance of ITO.

Figure 1c depicts the transfer characteristics of the device with a drain-source voltage (V_{ds}) of 0.01 V. The gate voltage (V_g) is swept from –10 to +10 V and then +10 to –10 V leading to a very large clockwise hysteresis related to the trapped electrons. The memory window width is approximately 9 V and the ON/OFF current ratio at V_g = 0 V is more than 10^3. As shown in Figure 1d, the measured currents for both program and erase states are very stable with a program/erase current ratio of approximately 10^3 over a duration of 600 s. After 600 s, both currents exhibit insignificant change for these two states, demonstrating a negligible charge leakage from the existing floating-gate. As a comparison, devices without the charge trapping layer were also fabricated and shown in Figure S2

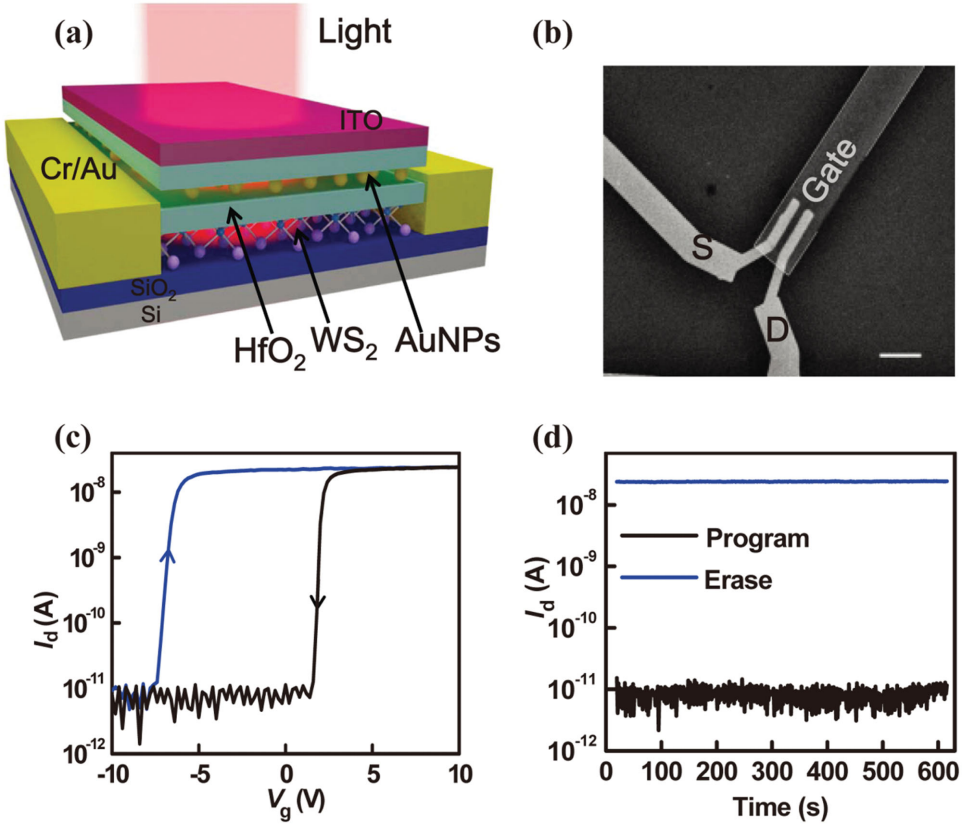

Figure 1. Device structure and preliminary electrical characterization of the WS_2 phototransistor with gold nanoparticles (AuNPs) embedded in the gate dielectric. a) 3D schematic view of the fabricated device. b) The top-view SEM image of the corresponding device. The scale bar is 5 μm. The channel width is 1.1 μm. c) Transfer characteristics of the floating-gate phototransistor based on multilayer WS_2 under dark at room temperature. d) The source-to-drain currents of the program/erase state over a hold time of 600 s. The voltage pulse duration is 3 s.

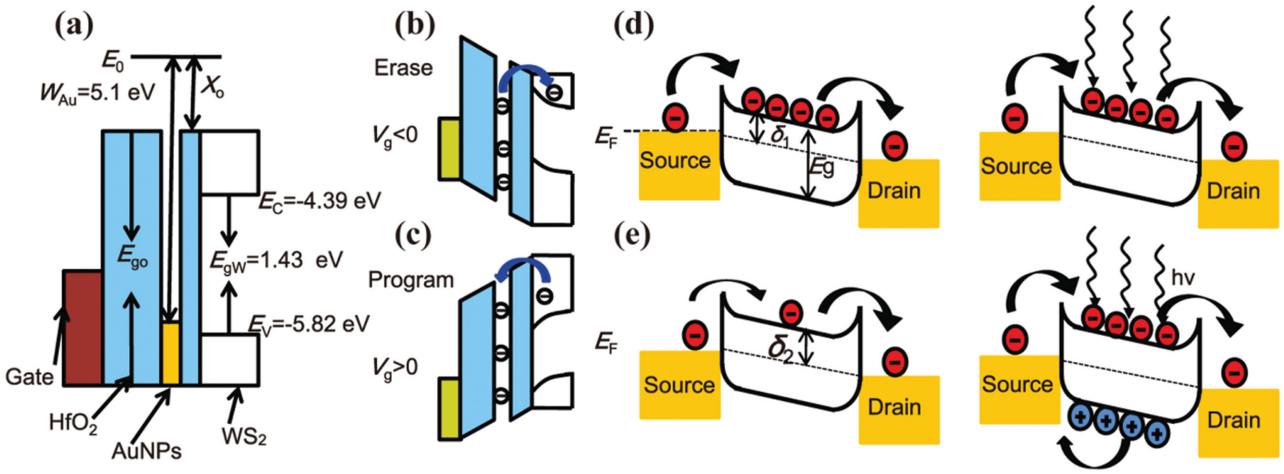

Figure 2. The working principle of the WS_2 phototransistor. a) Flat band state with no contact between layers. b,c) and d,e) Simplified schematic energy band diagrams at the two different states with and without illuminations showing the photocurrent generation process. E_F is the Fermi level and δ represents the height from the Fermi level to the bottom of conduction band related to the different states. W, E_g, E_0, and X_0 stand for the work function, band gap, electron affinity, and vacuum level, respectively. A relatively low voltage (0.01 V) is based between source and drain, and the gate voltage is kept at zero (V_g = 0 V).

in the Supporting Information. It is evident that there is no memory effect, indicating limited charge trapping in HfO_2 and the interface layers.[38] At the same time, these results further reveal that AuNPs sandwiched between two dielectric layers play a crucial role in suppressing the dark current of the phototransistor.

2.2. The Schematic Diagram of the Phototransistor

Moreover, operations of the phototransistor based on our floating-gate memory structure can be explicitly explained by a simplified energy band diagram as shown in **Figure 2**. By employing the floating-gate memory structure, there are two distinct resistive states of the WS_2 phototransistor used to describe the device operation: without the memory state (namely the erase state) and with the memory state (the program state). Importantly, these two states can be switched independently via suitable gate voltages, which can push the electrons back and forth between the floating-gate (AuNPs) layer and the WS_2 device channel. In the erase state, since there is a large I_d flowing across the channel by a source/drain bias under equilibrium, no charge is stored in the floating-gate. In order to save energy and maintain the device stability, the V_g is set to be 0 V. After illumination, the photogenerated current and dark current, including both thermionic and tunneling currents, also contribute to the device total current. It is noted that these thermionic and tunneling currents are almost at the same level of magnitude as the photogenerated current for a photoconductive transistor with two typical Schottky barriers[39] at the source and drain contacts as displayed in Figure 2c. As a result, these thermionic and tunneling currents are not negligible[40] which is the main reason that most photoconductive transistors suffer from a low signal-to-noise ratio as well as low sensitivity. On the other hand, the barrier height for electrons to tunnel through the tunneling oxide is the electron affinity difference between WS_2 and HfO_2. Once a suitable positive gate voltage (e.g., 10 V) is applied, the tunneling oxide energy band would slope downward therefore thinning the barrier. Hence, due to the Fowler–Nordheim tunneling effect, electrons tunneling from the conduction band of WS_2 through the HfO_2 oxide to the AuNPs would act as a large negative voltage function causing the conduction band of WS_2 to bend upward, thus resulting in the depletion of the intrinsic carrier concentration. In this case, the photocurrent becomes significant and dominant under illumination in the program state. Simultaneously, the illumination photons also induce a few tunneling electrons to be excited to the conduction band of HfO_2 and then fall back to WS_2, which weakens the negative voltage function and results in a slight increase in the intrinsic carrier concentration. Consequently, this would lead to the larger channel current by suppressing the dark current, thus enhancing the performance of photodetection.

2.3. Optical Characterization of the WS_2 Phototransistor

The corresponding device performance, **Figure 3**a, shows the output characteristics under illumination at a wavelength of 520 nm with a zero V_g in the program state. The obtained current is significantly increased under this irradiation as compared with the dark current (i.e., I_{light}/I_{dark} current ratio $\approx 10^3$), implying a high sensitivity to the incident light. The inset in the Figure shows the output characteristics in the erase state under dark and illumination conditions, respectively. It is obvious that the curves are linear for low bias voltages. Due to the low power density and large intrinsic carrier concentration, the dark current (10^{-8} A) is found to be three orders of magnitude higher than that of the program state (10^{-11} A). Therefore, it is difficult to distinguish between the dark and photogenerated currents. These findings clearly demonstrate that phototransistors based on our floating-gate memory

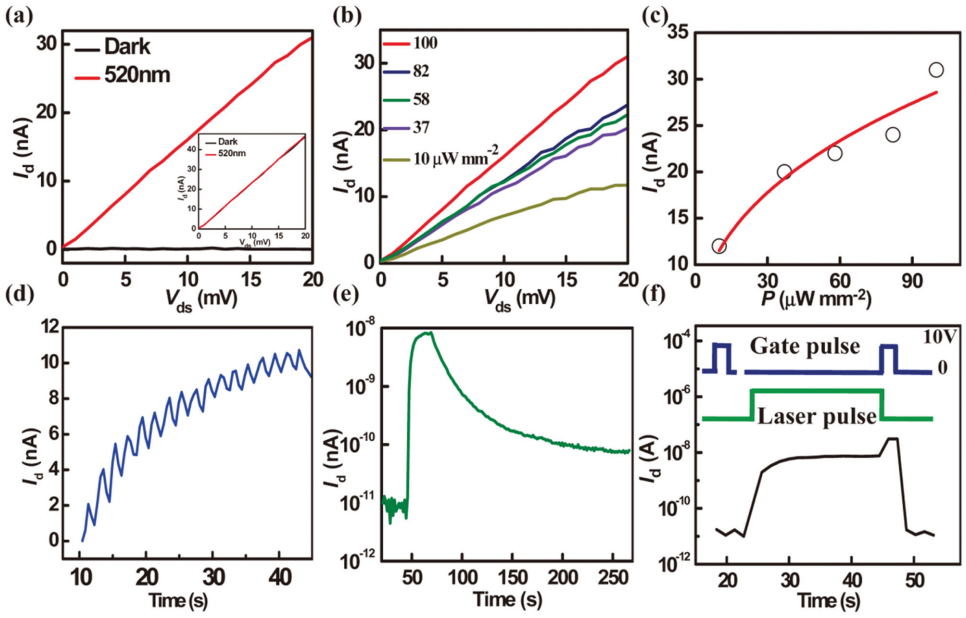

Figure 3. Optoelectronic characteristics of the WS_2 phototransistor based on the floating-gate memory structure. a) Output characteristics of the device with and without illumination in the program state. The inset shows similar measurements in the erase state with the illumination power density of 100 μW mm^{-2}. b) Output characteristics of the device at $V_g = 0$ V with memory functionality under different illumination powers. c) The incident power dependence of the device channel current. d) Normalized current response at continuous on/off cycles of light illumination with the on time of 1 s and the off time of 1 s. e) Time-resolved photoresponse of the phototransistor at one particular on/off illumination cycle. f) Time-resolved photoresponse of the device at an incident power of 100 μW mm^{-2} with a reset gate voltage pulse. The wavelength of the illumination is 520 nm.

structure have much better performance than conventional devices.

Figure 3b illustrates output characteristics with different illumination powers under the same wavelength in the device program state. With increasing light intensity, more electrons are excited into the conduction band and are then extracted by V_{ds} forming a large channel current. Figure 3c shows the corresponding I_d curve as a function of the laser power at V_{ds} = 0.02 V. The channel current rises with the increase in light intensity and yields a nonlinear relation, which fits the power law of $I = cP^k$, where c is a proportionality constant, P is the light intensity, and k is an empirical value. This can be explained in terms of the multifaceted processes of photogenerated carriers, similar to MoS_2-based phototransistors.[40] According to Figure 3c, the responsivity (R) and detectivity of the phototransistor are found to approach 1090 A W^{-1} and 3.5 × 10^{11} Jones, respectively, under a low illumination power density of 10 μW mm^{-2}, in which V_{ds} is 0.02 V, P is 10 μW mm^{-2}, R is given by I_p/P. I_p designates the photocurrent in the a detector while P represents the power density of illumination. Notably, this responsivity of 1090 A W^{-1} is already larger than the previously record result of 884 A W$^{-1,}$ which was measured in NH_3 atmosphere with V_g = 0 V, V_{ds} = 1 V, and P = 50 mW cm^{-2}. In addition, assuming that noise is the major factor in the dark current (Figure S5, Supporting Information), the detectivity can be given as $D^* = RA^{1/2}/(2eI_d)^{1/2}$, where R is the responsivity, A is the area of the detector, e is the charge of an electron, and I_d is the dark current.[41,42] In this work, an impressively high detectivity of 3.5 × 10^{11} Jones has been achieved, indicating that the proposed device is extremely sensitive to incident illumination. Moreover, there are similar studies reported of higher gain for other layered materials.[43–46]

Apart from the steady state behavior, transient response is another important characteristic for high-performance phototransistors. Figure 3d illustrates the channel current response of the device when characterized under on/off cycles of light illumination. It is seen that the time dependent photoresponse of the detector is not unusually fast but is acceptable. In order to understand the entire process as well as the mechanism, the transient photoresponse of the device is focused to measure one detailed on/off cycle as shown in Figure 3e. The channel current increases with illumination time (i.e., light-on) and the ratio of I_{light}/I_{dark} is approximately 10^3. However, when the illumination is absent, the dark current cannot return to its initial value efficiently but rather it slowly decreases. This result indicates that the illumination (wavelength, λ = 520 nm) causes electrons to be trapped by the AuNPs, thus exhibiting a slight leakage with the ratio of $I_{light}/I_{dark} \approx 10^2$ and leading to a slight increase in the resulting dark current value as shown in Figure 2. The number of leakage electrons is related to the duration of the illumination, as shown in Figure S2 in the Supporting Information. Also, the WS_2 trapping effect may have a significant impact on the device response time. It can be explained that the photoinduced electrons are excited to some of the trap states and remain trapped for a rather long time, which leads to the result that lifetimes of the excited holes, τ, in WS_2 are quite long. The corresponding response can be demonstrated by a typical rise time of t_{rise} = 6.98 s and decay time

of t_{decay} = 10.73 s for V_{ds} = 0.01 V and a zero V_g in the program state, where the rising and delayed segments of the curve can be fitted by using a single exponential function. A similar phenomenon, which is also attributed to the traps, is observed in monolayer MoS_2, hybrid graphene-quantum dot and amorphous oxide phototransistors as previously reported.[40,47,48]

For the sake of resolving the issue of insufficient response time, a gate pulse of 10 V is applied at the illumination-off stage. As depicted in Figure 3f, it is obvious that I_d decreases rapidly with the pulse duration. The relation between recombination rate and carriers under dark is governed by $|dn/dt| = n/\tau$, where n is the carrier concentration, τ is the lifetime of minority carriers, and $|dn/dt|$ is the recombination rate. It may be explained that the positive gate voltage can make the conduction band bend downward, thus increasing the carrier concentration. The instantaneous increase of carriers would increase the recombination rate, which accelerates the discharge of trapped charge carriers and results in a decrease in the photocurrent decay time for the device. Simultaneously, the device can be forced back into the program state, avoiding the different dark current value from cycles to cycles. This demonstrates that phototransistors based on the floating-gate memory structure can achieve the conventional electrical-light-electrical operating mode.

2.4. The MoS_2 Phototransistor Based on the Floating-Gate Memory Structure

To further explore the versatility of our floating-gate memory structure, we also demonstrate floating-gate phototransistors based on multilayers MoS_2 as shown in **Figure 4**. The channel width and channel length are fabricated as 4 and 1 μm, respectively. Figure 4a displays the two distinct operating states of the MoS_2 phototransistor, where the dark current can be significantly suppressed in the program state. Figure 4b illustrates the device output characteristics for different illumination powers, while Figure 4c,d proves that a similar method can be employed as well to force the photo-induced carriers into recombining after the illumination-off stage. Importantly, the photoresponsivity is up to 59.2 A W^{-1} at a wavelength of 520 nm under a low bias voltage of 0.02 V, a zero gate voltage and a power density of 0.55 mW mm^{-2}. The corresponding transfer characteristics and hold time response are shown in Figure S3 in the Supporting Information. The low responsivity of MoS_2 can be explained by the different thickness (note that the thickness of WS_2 is thicker than that of MoS_2) of the two different materials, thus the material thickness influences light absorption.[5] Moreover, the absorption of WS_2 is greater than that of MoS_2 at the same thickness.[20] These have experimentally confirmed that the floating-gate memory structure is indeed applicable to a variety of 2D materials for high-performance phototransistors.

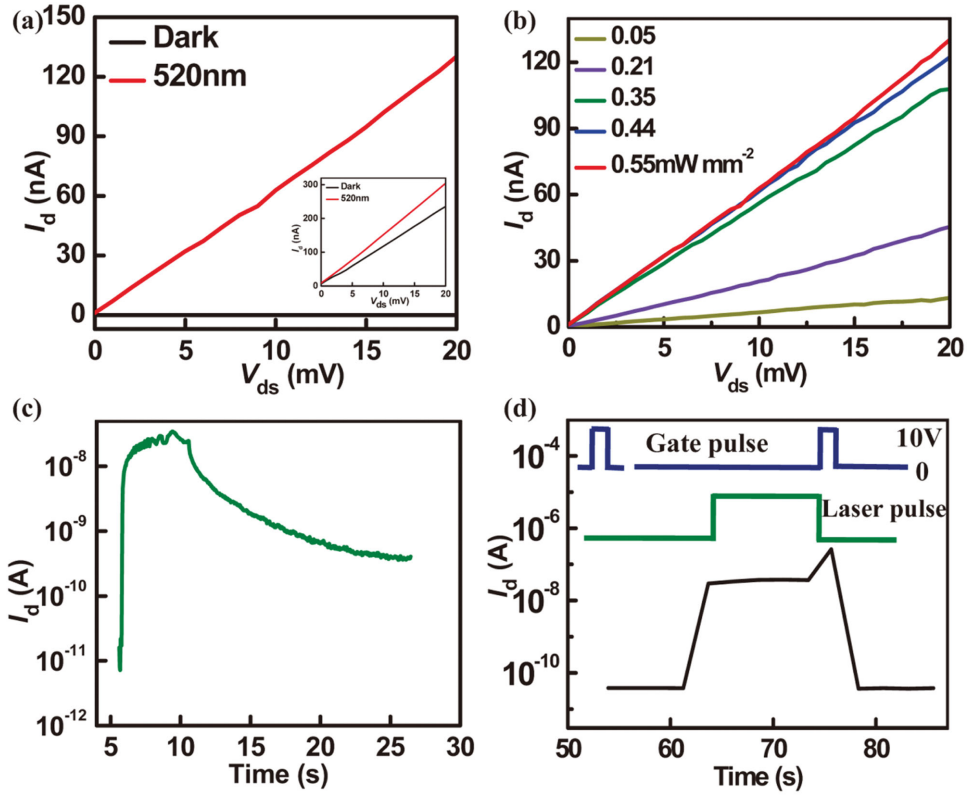

Figure 4. Optoelectronic characteristics of the few-layer MoS_2 phototransistor based on the floating-gate memory structure. a) Output characteristics of the device with and without illuminations in the program state. The inset image shows the output characteristics in the erase state with the illumination power density of 0.55 mW mm^{-2}. b) Output characteristics of the device under different illumination powers. c) Current response of the phototransistor for one particular on/off cycle of light illumination. d) The time response measurements of the MoS_2 phototransistor are dealt with as the same procedures and conditions as the WS_2 phototransistor.

3. Conclusion

In summary, the floating-gate memory structure and 2D materials are combined and utilized together for the realization of high-sensitivity and energy-saving phototransistors. The WS_2 floating-gate phototransistor not only exhibits respectable memory properties, including the large memory window and hold time, but also displays excellent photodetection capabilities in the program state. The high photoresponsivity of 1090 A W^{-1} and detectivity of 3.5×10^{11} Jones are achieved under a zero gate voltage and a small source/drain bias. Importantly, a similar floating-gate phototransistor based on another layered material, MoS_2, is also demonstrated to have improved performance as compared with conventional phototransistors, illustrating the versatility of the floating-gate memory structure investigated here. These impressive results indicate the technological potential of WS_2 and MoS_2 based floating-gate memory structures for the development of future phototransistor devices.

4. Experimental Section

Phototransistor Fabrication: Multilayer WS_2 and MoS_2 were mechanically exfoliated from commercially available crystals (purchased from SPI supplies). The layers were distinguished by observation under optical microscopy and Raman spectroscopy on a 255 nm thick SiO_2 dielectric layer thermally grown on top of a highly doped p-type Si substrate. The substrates were spin-coated with methyl methacrylate (MMA) and polymethacrylate (PMMA), and EBL (JEOL 6510 with Nanometer Pattern Generation System (NPGS)) was employed to define the source, drain, and gate patterns. After the lift-off process, a tunneling oxide (HfO_2) was deposited by ALD at 95 °C before 1 nm thick Al was deposited as the seeding layer. Next, 1 nm thick AuNPs was deposited by thermal deposition. A blocking oxide HfO_2 was formed by ALD followed by the deposition of the thick ITO achieved by magnetron sputtering at room temperature as the control gate. Finally, the device was thermally annealed at 200 °C for 2 h.

Characterization: Tunneling and blocking oxides were grown with a KE-MICRO TALD-200A machine. The gold nanoparticles were deposited by thermal deposition under a vacuum of 6×10^{-4} Pa and the image was obtained by a Bruker Multimode 8 with Scan Assist-Air probe under the peak force mode in ambient conditions. The control gate ITO was deposited by JSD300-IIMagnetron Sputtering after electron-beam lithography and a conventional lift-off process. The electrical and optoelectronic characterization were performed in vacuum at room temperature using a Lake Shore probe station. The photoresponse to laser excitation measurements employed a focused laser beam (λ = 520 nm) from a Single Mode Fiber-Pigtailed LP520-SF15.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

F.G., W.L., J.W. contributed equally to this work. W.H. and L.L. conceived and supervised the research. F.G. fabricated the devices. F.G., W. Luo, and P.W. performed the measurements. W.H., L.L., and F.G. wrote the paper. All authors discussed the results and revised the manuscript. The authors thank James Torley from the University of Colorado at Colorado Springs for critical reading of the manuscript. This work was partially supported by the Major State Basic Research Development Program (Grant No. 2014CB921600), Natural Science Foundation of China (Grant Nos. 11322441, 61290301, 61574101, and 61574152), Fund of Shanghai Science and Technology Foundation (Grant No. 14JC1406400), CAS Interdisciplinary Innovation Team, and Ten Thousand Talents Program for Young Talents.

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