Tunable Electronic Transport Properties of Metal-Cluster-Decorated III–V Nanowire Transistors

*Ning Han, Fengyun Wang, Jared J. Hou, Sen Po Yip, Hao Lin, Fei Xiu, Ming Fang, Zaixing Yang, Xiaoling Shi, Guofa Dong, Tak Fu Hung, and Johnny C. Ho**

In the past decade, III–V semiconductor nanowire (NW) materials such as InAs, InP, and InGaAs have attracted enormous research attention due to their superior physical properties for next-generation electronics, sensors, and photonics.[1–9] In particular, single InAs NW field-effect transistors (FETs) have been demonstrated with extraordinary electron mobility in the range of 3000 to 10 000 $cm^2 V^{-1} s^{-1}$ dependent on the NW diameter,[10–12] and when configured in parallel array NW thin-film transistors (TFTs), they exhibit GHz device operation even fabricated on mechanically flexible substrates.[13] However, the majority of these III–V NW transistors all function in accumulation or depletion mode since it is necessary to deplete the intrinsically high free carrier concentration in the NW channel in order to achieve the device OFF state.[11,14,15] In general, FETs can be constructed in two distinct operation modes, namely depletion mode (D-mode) and enhancement mode (E-mode), and both device modes are needed for electronic circuits. At the zero gate bias, D-mode transistors exhibit a non-zero current while their E-mode counterparts operate with off current; as a result, E-mode devices are highly preferred for energy-efficient and large-scale circuit integration design as there is no need to apply a gate voltage to switch off the transistors.[16–18]

In order to control these device operation modes, several strategies have been extensively explored to vary the threshold voltage (V_{TH}) of different NW transistors. For example, the surface morphology of ZnO NWs can be manipulated to induce different surface trap densities to modulate their free carriers such that FETs fabricated with smooth NWs (minimal trap concentration) exhibit D-mode behavior with negative V_{TH}, while associated corrugated NWs (significant trap concentration) yield E-mode characteristics with positive V_{TH}.[19–21] Moreover, the deposition of Au nanoparticles on ZnO NW surfaces can also create nanoSchottky junctions, enhance the formation of the charged O_2 adsorbates, and cause unusually high surface band bending in shifting the V_{TH} and improving the photoresponse.[22–24] In addition to the surface-architecture control, the increasing amount of metal doping in In_2O_3 NWs has also been utilized to compensate the oxygen vacancies and reduce their carrier concentration shifting the V_{TH} positively to attain E-mode transistors.[18] On the other hand, very few reports are focused on high-mobility III–V NWs. Although the complicated gate-stack structure (i.e., metal wrap-gate with high work function) has been illustrated to move the V_{TH} of InGaAs vertical NWFETs,[5] this sophisticated device design may potentially restrict the practical implementation of III–V NWs in electronic devices, sensors, and others. Therefore, it is urgently required to develop an easy and effective method to controllably tune the V_{TH} as well as adjust the device working mode of III–V NWFETs for technological applications.

Here, instead of utilizing the complex NW gate-stack design, we present a facile and reliable scheme to control the device operation by manipulating the V_{TH} of n-type III–V NWFETs via a metal cluster decoration approach, which is based on the work function difference between the metal clusters deposited and the NW materials to modulate the carrier concentration in the device channel. For the low work function metal clusters (i.e., Al), free carriers are donated from the clusters to the n-type channel such that the V_{TH} is negatively shifted for the D-mode NW transistors, whereas for the high work function metal clusters (i.e., Au), free electrons are withdrawn from the n-type channel to positively move the V_{TH} to obtain E-mode NW devices. In this work, InAs, InP, and $In_{0.6}Ga_{0.4}As$ NWs grown by a solid source chemical vapor deposition (CVD) method[2,25–27] are employed as the representative III–V NWs in which the metal cluster decoration approach is demonstrated to controllably tune the device operation of single NW devices as well as NW parallel array transistors with minimal changes in other electrical properties such as the field-effect mobility (μ_{FE}). These D- and E-mode devices have also been configured together as logic inverters with excellent performances, which further elucidate the technological potency of this metal cluster decoration for nanoelectronic device fabrication.

The scanning electron microscopy (SEM) image of one typical InAs NWFET (after 1.0 nm thick Au and 20 nm thick Al_2O_3 deposition) is shown in **Figure 1**a, together with the schematic illustration of the global back-gated transistor configuration. The electronic performances of the InAs NWFET before and after the Au cluster decoration are depicted in Figure 1b. It is obvious that the InAs NWFET operates initially in the D-mode, as the device exhibits non-zero drain current at the zero gate voltage; however, the Au cluster decoration can effectively shift the V_{TH} positively and thus make the NWFET work

Dr. N. Han, Dr. F. Wang, J. J. Hou, S. P. Yip, H. Lin, F. Xiu, M. Fang, Dr. Z. Yang, Dr. X. Shi, G. Dong, T. F. Hung, Prof. J. C. Ho
Department of Physics and Materials Science and Centre for Functional Photonics (CFP)
City University of Hong Kong
83 Tat Chee Avenue, Kowloon
Hong Kong S. A. R., P. R. China
E-mail: johnnyho@cityu.edu.hk
Dr. N. Han, Dr. F. Wang, J. J. Hou, S. P. Yip, F. Xiu, Prof. J. C. Ho
Shenzhen Research Institute, City University of Hong Kong, Shenzhen, P. R. China

DOI: 10.1002/adma.201301362

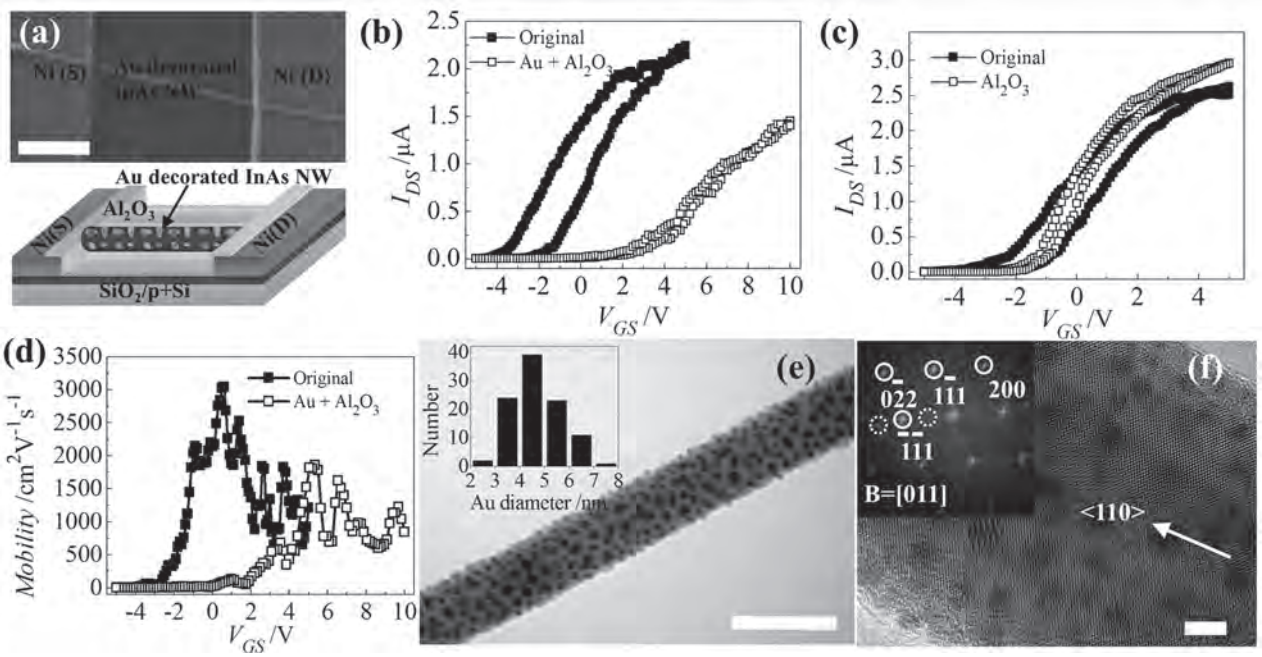

Figure 1. Au cluster decoration on InAs NWFETs. a) typical SEM image and schematic configuration of a Au decorated InAs NWFET (scale bar = 1 μm). b) I_{DS}–V_{GS} curves of the InAs NWFET before and after the decoration (decoration: Au cluster with an equivalent film thickness of 1.0 nm covered with a 20 nm thick evaporated Al_2O_3 layer; V_{DS} = 0.1 V). c) I_{DS}–V_{GS} curves of the InAs NWFET before and after Al_2O_3 deposition (control; V_{DS} = 0.1 V). d) Field-effect electron mobility of the InAs NWFET as a function of gate voltage before and after the Au cluster decoration (V_{DS} = 0.1 V). e) TEM image of the InAs NW after the decoration (scale bar = 50 nm) and inset is the diameter distribution statistic of decorated Au clusters. f) HRTEM image of the Au cluster decorated InAs NW (scale bar = 5 nm), and inset is the corresponding FFT.

in the E-mode. Quantitatively, as the square root of drain current ($I_{DS}^{1/2}$) is proportional to gate voltage ($V_{GS} - V_{TH}$), V_{TH} can be determined by the interpretation of the $I_{DS}^{1/2}$ –V_{GS} curve as shown in Figure S1, Supporting Information, where a V_{TH} shift of ≈4 V is obtained by the 1.0 nm thick Au decoration. In order to verify the effect of Al_2O_3 as a protective/passivation layer, another InAs NWFET with a similar NW channel dimension (diameter (d) ≈30 nm) is deposited with only a pure 20 nm thick Al_2O_3 layer as a control. As illustrated in Figure 1c, the Al_2O_3 layer cannot move the V_{TH} of the NWFET, instead it does reduce the device hysteresis by protecting the metal clusters from oxidation as well as passivating the NW surface from the ambient environment.[28] In this case, the role of Au cluster decoration is experimentally demonstrated to increase the V_{TH} of InAs NWFETs and transform the device operation from D-mode to E-mode.

To further explore the effect of Au cluster decoration on other electronic properties of InAs NWFETs such as μ_{FE}, by using the equation ($\mu_{FE} = GL^2/(C_{OX}\ V_{DS})$, where G is the transconductance (dI_{DS}/dV_{GS}), L is the NW channel length, C_{OX} is the gate oxide capacitance, and V_{DS} is the drain voltage), the μ_{FE} as a function of V_{GS} can be estimated before and after the decoration (Figure 1d).[11,29] It is clear that the original InAs NWFET has a peak mobility of ≈3000 $cm^2\ V^{-1}\ s^{-1}$, but decreases to ≈1800 $cm^2\ V^{-1}\ s^{-1}$ after the Au cluster deposition. Since the Au metal has a work function of 5.31–5.47 eV depending on the Au orientation, which is higher than the Fermi level of intrinsically n-type InAs (≈5.0 eV),[30] the free electrons would then get withdrawn from InAs once the Au and NW are in contact. This way, the free electron concentration, n, can also be qualitatively approximated on the order of 10^{18} cm^{-3} and decreased by <0.8 times before and after the decoration (summarized in Table S1, Supporting Information). All this reduction can be attributed to the existence of the 5–10 nm thick Au cluster induced depletion layer (see Supporting Information) that exists in the NW surface, reducing the effective NW channel width, enhancing the interface scattering, and thus lowering the μ_{FE}. In fact, in our previous study, the μ_{FE} of the NWFET was decreased by ≈0.6 times when the NW diameter was reduced by 10 nm.[11] At the same time, to examine the effect induced by the insertion of the top Al_2O_3 layer in the mobility calculation due to the enhanced coupling effect with both the back and top dielectric,[31] we carried out a control experiment with only 1.0 nm Au decoration without any Al_2O_3 layer in Figure S1, Supporting Information. It is clear that the mobility value obtained is similar while the hysteresis is not as minimized as the case with the Al_2O_3 layer, which again indicates the role of this Al_2O_3 film only as a passivation/protective layer. Although this passivation layer can simply improve the mobility by reducing the nanowire surface/interface recombination as shown in Figure 1c, as the surface depletion layer exists in the Au cluster decorated NWs and the film quality of the evaporated Al_2O_3 layer is not as good as the typical atomic layer deposited films, the capacitive coupling effect might be minimal and insignificant here.

It should also be noted that the effect of metal cluster decoration on NWFETs is observed to depend on the NW diameters. As shown in Figure S1, Supporting Information, the modulation of V_{TH} in InAs NEFETs is more pronounced in the thinner

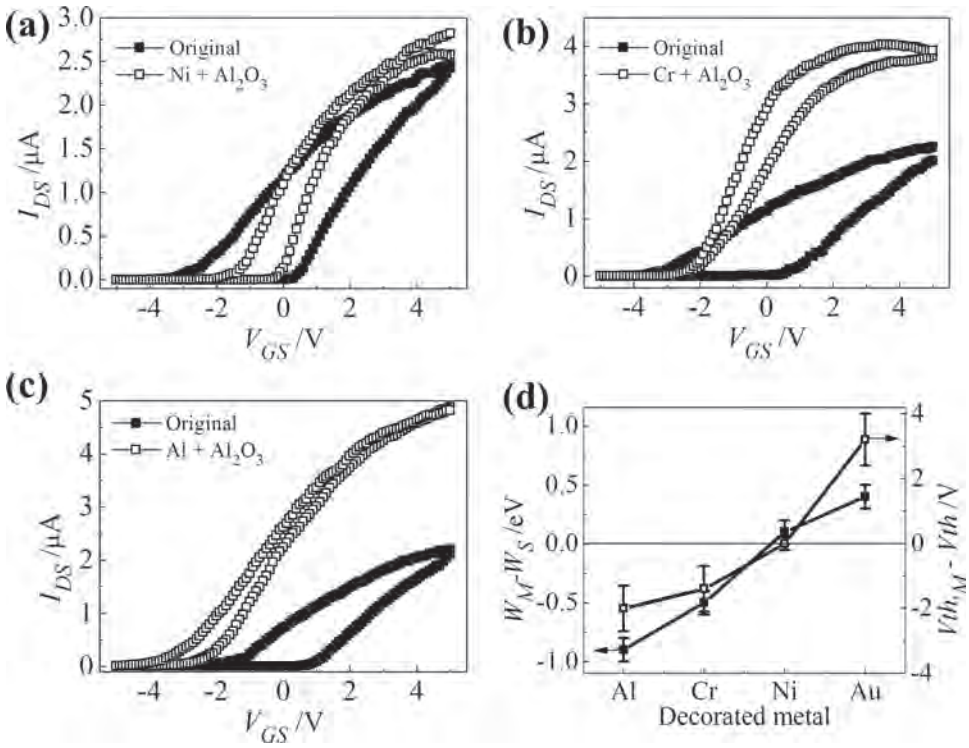

Figure 2. Effect of other metal cluster decoration (1.0 nm equivalent metal film thickness by thermal evaporation) on the electronic transport properties of InAs NWFETs: a) Ni, b) Cr, and c) Al. In order to prevent the oxidation of the metal, a 20 nm thick Al_2O_3 protection layer is also deposited by e-beam evaporation in the same chamber after the metal cluster decoration. d) Summary of the V_{TH} shift as a function of the work function difference of the metal and InAs.

NWs ($d \approx 20$ nm) as compared to the thicker NWs ($d \approx 40$ nm). Due to the nature of the extremely large surface-to-volume ratio in the NWs, the surface depletion induced by the Au clusters is believed to be more dominant for the thin NWs such that a larger magnitude of the positive V_{TH} shift is observed in the FETs. On the other hand, there exists an optimal thickness of the Au cluster film in this V_{TH} tailoring. When the Au clusters are too large as a result of the deposition of thicker films, the clusters start to aggregate to form a continuous film/mesh turning the NW metallic, while the clusters are too small from the thinner films, as such the V_{TH} tuning of FETs is not as effective (data not shown). In order to investigate the structural details of this optimal 1.0 nm thick equivalent Au cluster film deposited onto the InAs NWFETs, the clustered NWs without the protective Al_2O_3 are dispersed onto copper grids for transmission electron microscopy (TEM) imaging. As depicted in Figure 1e, these Au clusters are indeed individual and form discrete nanoparticles surrounding the NW surface with a diameter distribution of 4.7 ± 1.0 nm. These nanoparticles as well as the NW are then further characterized by high resoution (HR) TEM (Figure 1f), where the crystal lattice of the InAs NW is obviously shown, having a <110> orientation as confirmed by the fast Fourier transform (FFT) in the inset, but the lattice of Au clusters is not clearly observed (only the dashed circled spots in the FFT) due to the relatively low lattice amount of Au in the dominant InAs lattice background. The Au clusters were also directly deposited onto the carbon film (copper grid) and analyzed by TEM to mimic the crystallographic characteristics of these clusters deposited on NWs (Figure S2, Supporting Information). The Au nanoparticles are in fact polycrystalline as illustrated in the FFT (inset) having mixed crystal orientations with a work function spanning from 5.47 [Au(100)], 5.37 [Au(110)], to 5.31 eV [Au(111)];[30] therefore, the work function of these polycrystalline Au clusters is validated as 5.4 eV in this study.

In an effort to shed light on the effect of metal cluster decoration with other work functions, Ni, Cr, and Al clusters are also deposited with the same decoration approach on InAs NWFETs to investigate the changes in electronic transport properties of the NWs. Importantly, the NW device channel is chosen to be around 30 nm in diameter in order to perform a consistent comparison here. As presented in **Figure 2**a, since Ni has a work function of 5.04–5.35 eV depending on the crystal orientation, which is similar to that of our InAs NWs, the Ni cluster decoration is expected to play a negligible role in shifting the V_{TH} of InAs NWFETs. In contrast, Cr and Al have much lower work functions as compared to the InAs NWs (4.5 eV for Cr and 4.0–4.26 eV for different orientations of Al);[30] once these clusters are in contact with the NWs, free electrons are anticipated to donate to the NWs to enhance the transistor on-current as well as to shift the device V_{TH} negatively to D-mode operation, which is indeed supported by the electrical measurement results (Figure 2b and c). As such, similar to the Au cluster case, the corresponding free electron concentration, n, can be also estimated and it is found that there is an ≈2 times increase in the concentration, while the μ_{FE} improves slightly

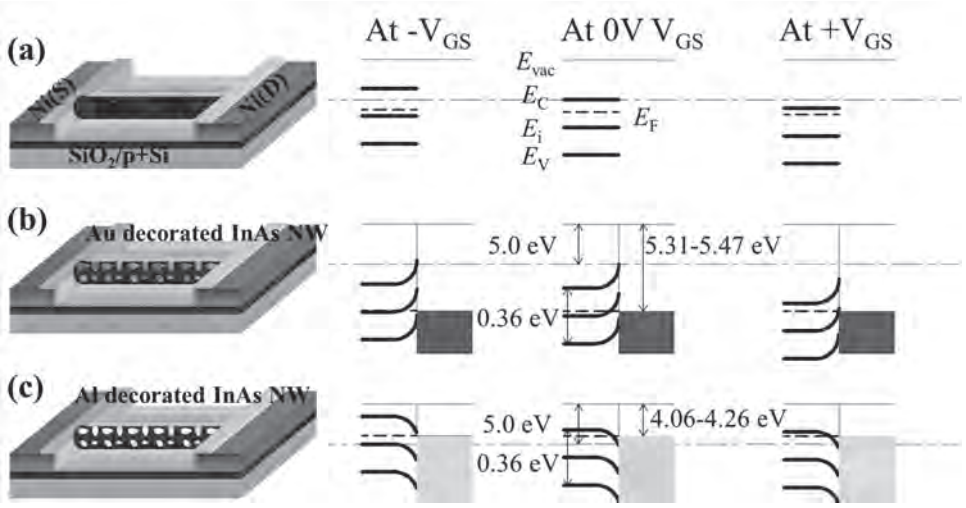

Figure 3. NWFET schematic illustration with different metal cluster decoration and the corresponding energy band diagram at different gate bias: a) bare InAs NW channel without any decoration, b) Au cluster decoration to positively shift the device V_{TH} (E-mode operation) by depleting the free electrons, and c) Al cluster decoration to negatively shift the device V_{TH} (D-mode operation) by donating the free electrons.

to ≈5000 cm^2 V^{-1} s^{-1} after the Cr and Al cluster decoration (Figure S3 and Table S1, Supporting Information). This mobility enhancement is believed to come from the reduction of the NW surface trap density and surface recombination induced by the top Al_2O_3 passivation layer.[11,28,32] Notably, this protective layer is essential for the metal cluster decoration of NWFETs as these metals (Cr and Al) are easily oxidized. As a result, the effect of metal cluster decoration on the V_{TH} modulation of InAs NWFETs is determined to depend on the work function difference between the metal (W_M) and NW (W_S); a positive work function difference (e.g., Au cluster case) would shift the V_{TH} to the right for E-mode device operation while a negative work function difference (e.g., Al cluster case) would then move the V_{TH} to the left for D-mode device characteristics. These results are further verified by a number of NWFET devices (10 in every metal decoration case) as statistically shown in Figure 2d, and also by the large-scale NW parallel array devices (≈60 NWs assembled in the device channel) detailed in the following section.

Moreover, this metal cluster decoration approach can also be applied to other III–V NWs such as InP. Figure S4, Supporting Information, summarizes the effect of different metal cluster decoration, together with the work function difference between the metal (W_M) and NW (W_S), in tuning the V_{TH} of InP NWFETs ($d \approx 30$ nm). It is obvious that the results are consistent with the case of InAs NWs even though InAs and InP have different Fermi levels and other properties. Again, the positive work function difference would increase the device V_{TH} while the negative work function difference would decrease the V_{TH} correspondingly without significant changes in the μ_{FE} of InP NWs. In addition to the binary compound semiconductor materials, the V_{TH} of tertiary $In_{0.6}Ga_{0.4}As$ NWFETs can also be tailored by this simple metal cluster decoration scheme (Figure S5, Supporting Information). Therefore, this decoration method is generally workable to most III–V NWFETs in controllably adjusting the device V_{TH} and operation mode, but more importantly, other electronic properties such as electron mobility are not changed substantially by this V_{TH} modulation as summarized in Figure S1 and Table S1, Supporting Information.

To intuitively understand the physical mechanism of this metal cluster decoration, **Figure 3** shows the NW device schematics along with various metal clusters with the corresponding energy band diagram at different gate bias. Specifically, the prepared InAs NWs are intrinsically n-type with the Fermi level, E_F, lying near or slightly pinned above the conduction band edge at equilibrium (V_{GS} = 0 V) because of the relatively high free electron concentration induced from the NW surface defects;[33–34] therefore, a negative gate bias is required to move the bands up or push the E_F down in order to deplete the free carriers to achieve the device off-state, which is known as D-mode device operation (Figure 3a). However, as illustrated in Figure 3b, when the Au clusters are decorated onto the NW channel, due to the large positive work function difference ($W_M - W_S$), the equilibrium band diagram is locally disturbed to induce a upward band-bending at the Au/NW interface such that the free electrons are depleted to move the E_F down to the intrinsic level, E_i (V_{GS} = 0 V), causing a positive shift in the device V_{TH}. As such, the NW device would exhibit zero current at the off-state at a zero gate bias unless a positive gate bias is applied to push the bands down to extract the carriers (E-mode characteristics). On the contrary, when Al clusters are deposited, the negative $W_M - W_S$ would create a downward band-bending at the Al/NW interface so that free electrons are donated to the NWs leading to a higher on-current and a negative shift in the device V_{TH} (Figure 3c). All of these have further confirmed that the NW device V_{TH} and operation mode can be effectively tuned by this metal cluster decoration approach. It is also noted that this band model is only qualitative and a more thorough theoretical model is required to further quantify the effect and magnitude of this band-bending as well as the modulation of free carriers (device V_{TH}) with different metal clusters and NW diameters in the future.

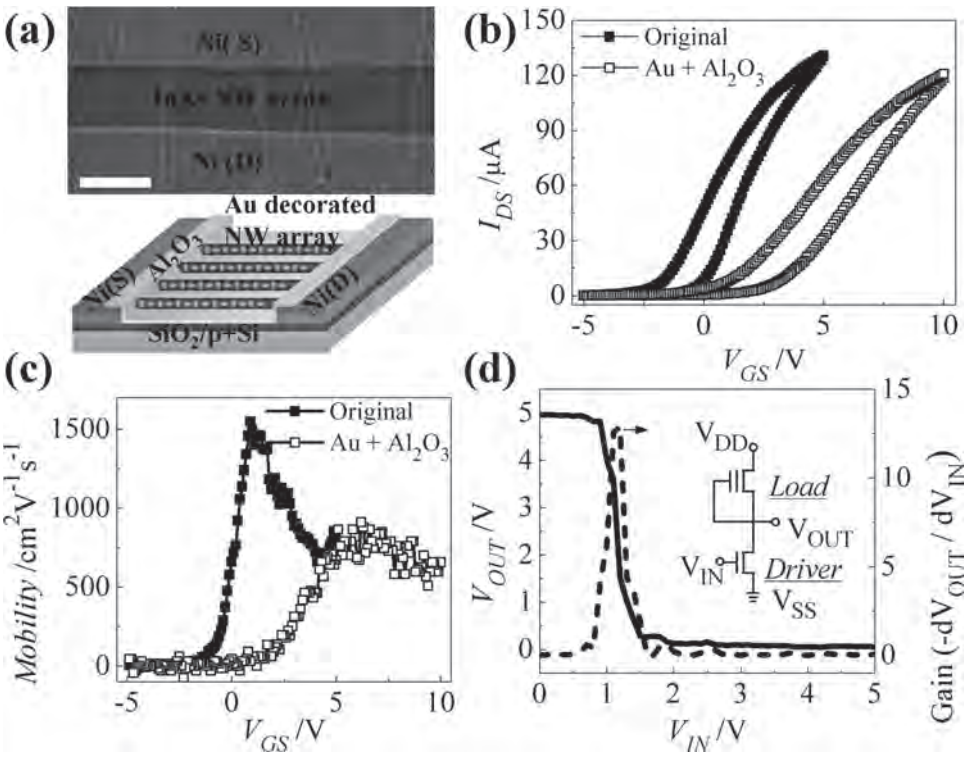

Figure 4. Application of the metal decoration method in transforming printed NW parallel array devices into E-mode and in the fabrication of NMOS inverters composed of an E-mode and D-mode NWFET. a) SEM image and schematic illustration of a Au cluster decorated InAs NW array FET, scale bar = 1 μm. b) $I_{DS} - V_{GS}$ curves before and after decoration (decoration: Au clusters with an equivalent film thickness of 1.0 nm covered with a 20 nm thick evaporated Al_2O_3 layer; V_{DS} = 0.1 V). c) Field-effect mobility of a InAs NW array FET before and after decoration (V_{DS} = 0.1 V). d) The voltage transfer characteristics (solid line) and the corresponding gain (dash line) of the representative NMOS inverter, the inset is the schematic circuit diagram of the inverter.

Apart from the single NW devices, utilizing the NW contact printing,[25,35] E-mode InAs NW parallel array FETs are also fabricated to illustrate the applicability of this metal cluster decoration approach for large-scale device integration. **Figure 4**a shows the SEM image and schematic of one representative device decorated with Au clusters in the NW channel. The printed FET has a device width of ≈30 μm and a channel length of ≈1.5 μm, while Ni source and drain electrodes are employed and configured in the global back-gate device geometry. Notably, the NW print density is observed as ≈2 NW μm^{-1} accounting for ≈60 NWs in the channel (Figure 4a inset). Considering an average current of ≈2 μA per NW at V_{DS} = 0.1 V, the device on-current is estimated as ≈120 μA, which is in good agreement with our electrical measurement (Figure 4b), indicating the excellent uniformity of our NW printing as well as the NW performances. More importantly, the NW parallel array FET is initially operating in the D-mode similar to the single InAs NWFET, but after the Au cluster decoration, the device V_{TH} is shifted positively to transform into an E-mode transistor. At the same time, on the basis of previous μ_{FE} calculation of single NW devices, the μ_{FE} of a NW parallel array FET (with the effective channel length of ≈1.5 μm) is not significantly scarified in this E-mode transformation. This slight reduction (≈0.5 times) in μ_{FE} is mainly attributed to the thinning of the effective NW channel due to the formation of a surface depletion layer induced by Au clusters. In any case, the obtained μ_{FE} (≈800 $cm^2\ V^{-1}\ s^{-1}$) as shown in Figure 4c already outperforms state-of-the-art Si and metal oxides for TFT applications. In future, further improvement of the device performance could be expected by optimizing the NW density, reducing channel length, and using a top-gated structure with high-*k* dielectrics.

In order to further investigate the reliable control of the device V_{TH} achieved in this work, functional digital circuits have been constructed.[20,36] In this case, utilizing the metal cluster decoration approach, we have demonstrated n-channel metal oxide-semiconductor (NMOS) inverters which utilize a Au-decorated E-mode InAs NWFET driver ($d \approx 30$ nm) and an original D-mode InAs NWFET load ($d \approx 25$ nm) with gate and source/drain terminals connected as depicted in Figure 4d (inset) and the Supporting Information. The transfer curve in Figure 4d shows clearly that the input signal is inverted with a high gain ($-dV_{OUT}/dV_{IN}$) of ≈13. Notably, the inverter can be operated effectively with a 100 Hz, 5 V square waveform input as illustrated in Figure S6, Supporting Information, while the ultimate performance limit is still under investigation. More importantly, due to the high electron mobility and low operating voltage of these InAs NWs, the power dissipation of this III–V NW NMOS inverter is found to be respectively low as compared to the thin-film ones. Specifically, there is no power consumed at 0 V input as a result of the "OFF" state of the driver; on the other hand, the output current at 5 V input is the saturation current of the load at 0 V gate bias (≈0.8 μA as shown

in Figure S6, Supporting Information). As such, the static power dissipation is estimated to be as low as ≈4 μW, which is comparable to the lowest NW NMOS reported values and far lower than their planar counterparts.[37,38] Further performance enhancements can also be achieved with the optimized device geometry with a top-gated structure for the smaller parasitic capacitance.

In summary, we have presented a facile and reliable approach to tailor the device operation of III–V NWFETs via metal cluster decoration, which can effectively modulate the transistor V_{TH} with minimal changes in device performance by simply controlling the work function difference between metal clusters and NWs. Specifically, since Au metal has a higher work function than most III–V NWs, its cluster decoration would shift the device V_{TH} positively to transform into E-mode operation, while the Al counterpart has a much lower work function that would negatively move the device V_{TH} to exhibit D-mode behavior. Meanwhile, high-performance E-mode InAs NW parallel array FETs are fabricated and decorated with Au clusters to demonstrate the applicability of this metal cluster decoration scheme to large-scale device processing. Furthermore, inverters based on both D- and E-mode metal decorated NWFETs are also configured to illustrate the reliable control of device V_{TH} for device integration. All these have indicated the great potency of the metal cluster decoration approach for future high performance, low power nanoelectronics, sensors, and their device fabrication.

Experimental Section

InAs, InP, and $In_{0.6}Ga_{0.4}As$ NWs used in this study were prepared by a solid source CVD method as previously reported.[2,25–27] Briefly, the source powders (99.999% purity) were heated in the upstream heating zone of a two zone tube furnace and the evaporated precursors were transported by a H_2 carrier gas flow (99.999% purity, 100 sccm) to the downstream heating zone. In this zone, NWs were grown by a Au catalyst film (0.5 nm in thickness) on SiO_2/Si substrates for 1 h. After naturally cooling in a H_2 gas atmosphere, the grown NWs were ultrasonically suspended into anhydrous ethanol solution, and then drop-cast onto SiO_2/Si substrates (50 nm thick thermal oxide) for FET fabrication and onto copper grids for TEM (Philips CM-20 and JEOL 2100F). The FETs were fabricated by a conventional lithography process and the 50 nm thick thermally deposited Ni films were used as the source and drain electrodes followed by metal lift-off. The selected metal clusters such as Au, Ni, Cr, and Al were then thermally deposited onto the FET device with an equivalent film thickness of 1.0 nm and a 20 nm thick Al_2O_3 layer was also deposited by e-beam evaporation in the same vacuum chamber to protect the metal clusters from oxidation. The electrical performance of the fabricated back-gated NWFETs was characterized with a standard electrical probe station connected with an Agilent 4155C semiconductor analyzer and SEM images of the FETs were taken using an FEI/Philips XL30.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

N.H., F.W. and J.J.H. contributed equally to this work. This research was supported by the General Research Fund of the Research Grants Council of Hong Kong SAR, China, under project numbers CityU 101210 and CityU 101111, the National Natural Science Foundation of China (grant number 51202205), the Guangdong National Science Foundation (grant number S2012010010725), the Science Technology and Innovation Committee of Shenzhen Municipality (grant number JCYJ20120618140624228), and was supported by a grant from the Shenzhen Research Institute, City University of Hong Kong.

Received: March 26, 2013
Revised: May 3, 2013
Published online: June 20, 2013

[1] W. I. Van, S. R. Plissard, E. P. Bakkers, S. M. Frolov, L. P. Kouwenhoven, *Nano Lett.* **2013**, *13*, 387.
[2] J. J. Hou, N. Han, F. Wang, F. Xiu, S. Yip, A. T. Hui, T. Hung, J. C. Ho, *ACS Nano* **2012**, *6*, 3624.
[3] J. Wallentin, M. Ek, L. R. Wallenberg, L. Samuelson, M. T. Borgström, *Nano Lett.* **2012**, *12*, 151.
[4] P. M. Wu, N. Anttu, H. Xu, L. Samuelson, M. E. Pistol, *Nano Lett.* **2012**, *12*, 1990.
[5] K. Tomioka, M. Yoshimura, T. Fukui, *Nature* **2012**, *488*, 189.
[6] J. A. del Alamo, *Nature* **2011**, *479*, 317.
[7] A. M. Ionescu, H. Riel, *Nature* **2011**, *479*, 329.
[8] D. Spirkoska, A. F. i Morral, J. Dufouleur, Q. Xie, G. Abstreiter, *Phys. Status Solidi RRL* **2011**, *5*, 353.
[9] M. S. Gudiksen, L. J. Lauhon, J. Wang, D. C. Smith, C. M. Lieber, *Nature* **2002**, *415*, 617.
[10] C. Thelander, P. Caroff, S. Plissard, A. W. Dey, K. A. Dick, *Nano Lett.* **2011**, *11*, 2424.
[11] A. C. Ford, J. C. Ho, Y. L. Chueh, Y. C. Tseng, Z. Y. Fan, J. Guo, J. Bokor, A. Javey, *Nano Lett.* **2009**, *9*, 360.
[12] M. D. Schroer, J. R. Petta, *Nano Lett.* **2010**, *10*, 1618.
[13] T. Takahashi, K. Takei, E. Adabi, Z. Fan, A. M. Niknejad, A. Javey, *ACS Nano* **2010**, *4*, 5855.
[14] Y. Huang, X. Duan, Y. Cui, C. M. Lieber, *Nano Lett.* **2002**, *2*, 101.
[15] S. A. Dayeh, D. P. R. Aplin, X. Zhou, P. K. L. Yu, E. T. Yu, D. Wang, *Small* **2007**, *3*, 326.
[16] B. Nikoobakht, *Chem. Mater.* **2007**, *19*, 5279.
[17] Y. Xuan, Y. Wu, P. Ye, *IEEE Electron Dev. Lett.* **2008**, *29*, 294.
[18] X. Zou, X. Liu, C. Wang, Y. Jiang, Y. Wang, X. Xiao, J. C. Ho, J. Li, C. Jiang, Q. H. Xiong, L. Liao, *ACS Nano* **2013**, *7*, 804.
[19] W. K. Hong, J. I. Sohn, D. K. Hwang, S. S. Kwon, G. Jo, S. Song, S. M. Kim, H. J. Ko, S. J. Park, M. E. Welland, *Nano Lett.* **2008**, *8*, 950.
[20] G. Jo, W. K. Hong, J. Maeng, M. Choe, W. Park, T. Lee, *Appl. Phys. Lett.* **2009**, *94*, 173118.
[21] W. K. Hong, D. K. Hwang, I. K. Park, G. Jo, S. Song, S. J. Park, T. Lee, B. J. Kim, E. A. Stach, *Appl. Phys. Lett.* **2007**, *90*, 243103.
[22] C. Y. Chen, J. R. D. Retamal, D. H. Lien, M. W. Chen, I. W. Wu, Y. Ding, Y. L. Chueh, C. I. Wu, J. H. He, *ACS Nano* **2012**, *6*, 9366.
[23] M. W. Chen, J. R. D. Retamal, C. Y. Chen, J. H. He, *IEEE Electron Dev. Lett.* **2012**, *33*, 411.
[24] M. W. Chen, C. Y. Chen, D. H. Lien, Y. Ding, J. H. He, *Optics Express* **2010**, *18*, 14836.
[25] A. C. Ford, J. C. Ho, Z. Y. Fan, O. Ergen, V. Altoe, S. Aloni, H. Razavi, A. Javey, *Nano Res.* **2008**, *1*, 32.
[26] A. T. Hui, F. Wang, N. Han, S. P. Yip, F. Xiu, J. J. Hou, Y. T. Yen, T. F. Hung, Y. L. Chueh, J. C. Ho, *J. Mater. Chem.* **2012**, *22*, 10704.
[27] N. Han, F. Y. Wang, A. T. Hui, J. J. Hou, G. C. Shan, F. Xiu, T. F. Hung, J. C. Ho, *Nanotechnology* **2011**, *22*, 285607.
[28] M. Huang, Y. Chang, C. Chang, Y. Lee, P. Chang, J. Kwo, T. Wu, M. Hong, *Appl. Phys. Lett.* **2005**, *87*, 252104.

[29] O. Hayden, M. T. Björk, H. Schmid, H. Riel, U. Drechsler, S. F. Karg, E. Lörtscher, W. Riess, *Small* **2007**, *3*, 230.
[30] D. R. Lide, *CRC Handbook of Chemistry and Physics* 90th ed., CRC press, Boca Raton **2010**.
[31] M. S. Fuhrer, J. Hone, *Nat. Nanotechnol.* **2013**, *8*, 146.
[32] S. Kim, P. D. Carpenter, P. K. Jean, H. Chen, C. Zhou, S. Ju, D. B. Janes, *ACS Nano* **2012**, *6*, 7352.
[33] J. Weber, A. Janotti, C. Van de Walle, *Appl. Phys. Lett.* **2010**, *97*, 192106.
[34] L. Olsson, C. Andersson, M. Håkansson, J. Kanski, L. Ilver, U. O. Karlsson, *Phys. Rev. Lett.* **1996**, *76*, 3626.
[35] Z. Y. Fan, J. C. Ho, T. Takahashi, R. Yerushalmi, K. Takei, A. C. Ford, Y. L. Chueh, A. Javey, *Adv. Mater.* **2009**, *21*, 3730.
[36] M. Yu, Y. Z. Long, B. Sun, Z. Fan, *Nanoscale* **2012**, *4*, 2783.
[37] A. Seyedi, A. Pavel, A. Sharma, N. Islam, *IET Micro Nano Lett.* **2009**, *4*, 16.
[38] A. Bindal, S. Hamedi-Hagh, *Semicond. Sci. Technol.* **2006**, *22*, 54.