

Manipulating III–V Nanowire Transistor Performance via Surface Decoration of Metal-Oxide Nanoparticles

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Recently, III–V semiconductor nanowires (NWs) are widely investigated as field-effect transistors (FETs) for high-performance electronics, optoelectronic, and others; nevertheless, effective control in their device performances, especially the threshold voltage is still not well attained, which can potentially limit their practical uses for technological applications. This study reports a simple but highly reliable metal-oxide nanoparticle (NP) surface decoration approach onto the device channel in order to manipulate electrical characteristics of III–V NWFETs, such as the threshold voltage and transistor operation, through the manipulation of free electrons in the NW channel (i.e., InAs, InP, and $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$) via depositing various metal-oxide NPs with different work functions. Without any passivation layer, this decoration approach can yield the stable NW device characteristics in ambient. Notably, the versatility of our decoration scheme has also been illustrated through the realization of high-performance enhancement-mode InAs NW-paralleled-arrayed devices as well as the configuration of highly efficient InAs NW NMOS inverters, comprising of both depletion and enhancement mode devices. All these results further elucidate the technological potential of this decoration approach for future high-performance, low-power nanoelectronic device fabrication, and circuit integration.

Particularly, InAs NWs have been demonstrated with the impressive field-effect electron mobility (μ_{FE}) of higher than $10000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ when configured into single nanowire field-effect transistors (NWFETs) as well as the highly efficient visible and near-infrared photoresponse at room temperature.^[2,3,9,11–13,19,20] Overall, field-effect transistors (FETs) can be configured into two separate operation schemes, which are known as enhancement-mode (E-mode) and depletion-mode (D-mode). Although these two schemes are complementarily needed for the design of advanced electronic circuits, at the zero gate bias, the E-mode transistor typically operates with an OFF current, while its D-mode counterpart gives a nonzero current such that a gate voltage is needed to deplete accumulated carriers to achieve the OFF state of devices. Therefore, the E-mode transistor is primarily preferred for the energy-efficient and large-scale circuit integration.^[14–17] However, most of

the III–V NWs consist of significant amounts of surface/interface traps, originating from the native oxide and/or unoptimal interface associating with high- κ dielectrics directly deposited on the top, which yield the accumulation layer on NWs' surface pinning the Fermi level above the conduction band or below the valence band.^[14,16–18] Even though the different diameter,

1. Introduction

In the past decades, due to their exceptional physical properties, high-performance III–V semiconductor nanowires (NWs) have been intensively studied and explored as fundamental building blocks for electronics, photonics, and sensors.^[1–10]

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DOI: 10.1002/admi.201700260

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/admi.201700260>.

surface trap density, morphology, doping concentration, and free carrier density, etc of the NWs would lead to variation in the device threshold voltage,^[14,17,19,20] these NWFETs (e.g., InAs) are mostly operated in the intrinsic D-mode domain.^[13,14,16,17]

In order to control the operation mode, several investigations have been recently performed to modulate the threshold voltage (V_{TH}) of different III–V NW devices.^[13,14,17,21] Tomioka et al. could manipulate the V_{TH} of InGaAs vertical NWFETs by using the unique configuration of wrapping gate with different metal choices; however, this sophisticated device design might potentially restrict their practical applications in electronic devices, detectors, and so on.^[21] At the same time, epitaxial InP thin-film shells were grown on InAs NW cores as the surface cap, which could be functioned to deplete electrons in the surface accumulation layer of InAs, shifting the device V_{TH} to the positive voltage direction for the E-mode operation, but requiring complicated metal-organic vapor phase epitaxy or chemical vapor deposition for the formation of these core/shell NW heterostructures.^[13] Instead of applying the complex NW gate-stack design and heterostructures, we have successfully controlled the device operation of III–V NWFETs via metal-cluster decoration in our previous work.^[14] In specific, the device V_{TH} could be effectively tuned by decorating the NW channel with different kinds of metal clusters. Based on the work function difference between the NW and the deposited metal clusters, the carrier concentration of device channels could be modulated accordingly. In any case, although this simple technique was demonstrated to vary the V_{TH} of different III–V NW transistors efficiently, these fabricated transistors had limited air stability due to the rapid oxidation of decorated metal clusters in the ambient environment. Therefore, a thin layer of Al_2O_3 was needed to passivate the metal clusters from oxidation, which could possibly limit their uses of NWFETs in certain application fields. In addition, we have as well employed thiolate-based aromatic monolayers with controllable molecular structure and electron density to modify the surface carrier concentration of InAs NW channels, resulting in manipulable changes of the device V_{TH} .^[17] Because of the sensitivity of these organic molecules to oxygen and humidity, this chemical passivation approach of NWFETs was again unstable in the ambient. It is also noted that since the electron withdrawing or donating effect of thiolate-based aromatic monolayers was limited, the resulting device V_{TH} could only shift with a relatively small range of 0.25 to 1.57 V.^[17] To date and to the best of our knowledge, neither of them has provided an ideal solution owing to their above-mentioned drawbacks. In this case, an effective, simple, and stable method to controllably modulate the V_{TH} and device operation of III–V NWFETs is still essentially needed for their further development of high-performance device applications.

Here, we propose and report a facile and practical technique to reliably control the III–V NW transistor performance via surface decoration of metal-oxide nanoparticles (NPs), which is relied on the work function difference between the NW material and deposited metal-oxide NPs in order to effectively modulate the carrier concentration of device channels. Explicitly, when the high-work-function metal-oxide NPs (e.g., CuO) are deposited onto the device channel, free electrons are withdrawn from the NWs to positively shift the device V_{TH} , achieving E-mode

device characteristics. On the other hand, when the low-work-function metal-oxide NPs (e.g. SnO_2) are decorated, free electrons are transferred from the metal-oxide NPs to the NWs, moving the V_{TH} toward the negative region for the D-mode device operation. In this work, binary NWs, such as InAs and InP, and ternary NWs of $In_{0.7}Ga_{0.3}As$ are selected as the representative III–V NWs in order to illustrate the effect of efficient V_{TH} modulation by different metal-oxide NPs (i.e., CuO, Ag_2O , NiO, and SnO_2) for both single NW and NW-paralleled-arrayed devices with good stability in the ambient. More importantly, other electrical properties or device parameters, including ON current and μ_{FE} , are not significantly changed with this approach. In addition, high-performance E-mode and D-mode NW-paralleled-arrayed transistors have also been assembled together as inverters with the impressive performance, which further illuminates technological potencies of this metal-oxide surface decoration scheme for the future nanoelectronic device fabrication.

2. Results and Discussion

In general, typical arsenic- and phosphide-based III–V NWs exhibit intrinsic n-type conductivity without any intentional doping, which could be originated from the donor-like crystal defects, such as the group V vacancy and/or group III interstitials.^[10] At the same time, due to the existence of large amounts of surface/interface states arising from the NW native oxide and/or unoptimal high- κ dielectric deposition on top of NWs, these electron-like trap states would induce an electron surface accumulation layer.^[13,14,17] All these would lead to the Fermi level (E_F) pinning above the conduction band and the subsequent D-mode operation of NW devices.^[13,14,17] In this investigation, the overall design concept of modulating III–V NW device characteristics is simple and the corresponding illustrative schematics are depicted in **Figure 1**. As predicted, when configured into the back-gated individual NW device, the as-prepared InAs NW demonstrates a typical n-type conductivity and D-mode device operation with the V_{TH} less than 0 V (Figure 1a,e). After CuO NPs are surface decorated onto the NW channel, the corresponding V_{TH} is positively shifted to greater than 0 V while the device operation is converted into the E-mode (Figure 1b,e). It is also noted that reliable control of these NP dimension and corresponding chemical composition is essential to the surface decoration. If the particle size is too large, the continuous conducting mesh would be resulted to affect the intrinsic NW conductivity; on the other hand, when the particle size is too small, the V_{TH} modulating effect would be insufficient. Moreover, if the decorated NPs are inhomogeneous in the composition, the resulting V_{TH} modulation would not be uniform, significantly deter its implementation for large-scale and practical device utilizations. Here, it is found that when starting with the Cu film of 0.5 nm in nominal thickness and successive thermal annealing of 120 °C for 20 min, it would yield the ideal and discrete surface decoration of NPs onto the device channel (Figure 1c,d). Notably, this relatively low temperature processing step does not affect adversely on the electrical contact properties of NWs. Based on the statistics of more than 80 individual NWs processed with

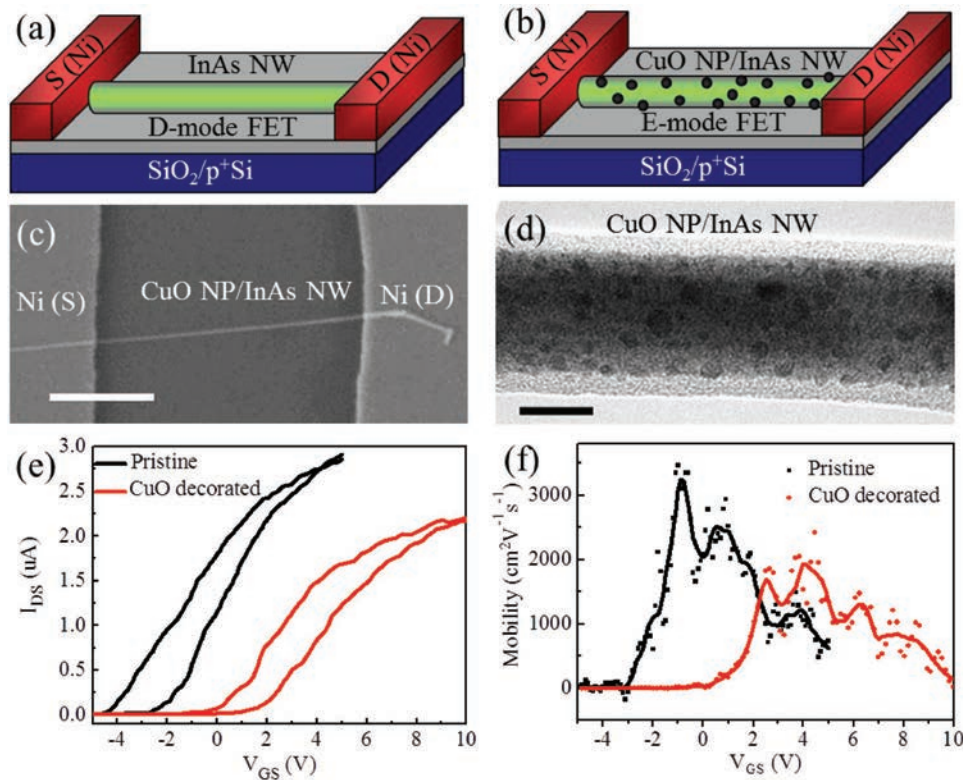


Figure 1. CuO NP decoration on InAs NWFETs. CuO NPs prepared by deposition of Cu film with the nominal thickness of 0.5 nm, followed by annealing at 120 °C for 20 min. a) Schematic view of a D-mode InAs NWFET. b) Schematic view of a E-mode InAs NWFET surface decorated with CuO NPs. c) Top-view SEM image (scale bar = 1 μm) of a representative E-mode InAs NWFET decorated with CuO NPs. d) TEM image (scale bar = 20 nm) of a typical CuO NP decorated InAs NW. e) $I_{\text{DS}}-V_{\text{GS}}$ curves at $V_{\text{DS}} = 0.1$ V for InAs NWFETs with the NW diameter of ≈ 30 nm, shown in (c), with and without the CuO NP decoration and f) the corresponding field-effect electron mobility as a function of the gate voltage.

this particular decorating condition, the average CuO NP size and InAs NW diameter are determined to be 4.6 ± 1.1 nm and 31.9 ± 6.0 nm, respectively, under electron microscopy (Figure 1c,d; Figure S1a,b, Supporting Information), while the chemical stoichiometry of NPs is confirmed to be homogeneous CuO with the appropriate X-ray photoelectron spectroscopy (XPS) peaks of Cu $2p_{3/2}$ and Cu $2p_{1/2}$ (Figure S1c, Supporting Information). In this case, for a typical NW diameter of ≈ 30 nm, the effect of these CuO NPs on the NW device characteristics can be illustrated by the shift of V_{TH} from ≈ -2.7 (i.e., undecorated) to 0.6 V (i.e., decorated), where the threshold voltages are determined by the interpretation of the $I_{\text{DS}}^{1/2}-V_{\text{GS}}$ curve (Figure 1e; Figure S2e, Supporting Information). This remarkable change of V_{TH} of 3.3 V in the positive gate-bias direction indicates evidently the effectiveness of metal-oxide NP surface decoration in reliably altering the NW device operation scheme. Besides, the μ_{FE} changes of these InAs NWFETs induced by the CuO NP decoration can also be evaluated using the equation

$$\mu_{\text{FE}} = g_{\text{m}} L^2 / (C_{\text{OX}} V_{\text{DS}})$$

where $g_{\text{m}} = dI_{\text{DS}}/dV_{\text{GS}}$ is the transconductance at a constant V_{DS} , L is the NW device channel length, C_{OX} is the gate oxide capacitance modeled from the finite element analysis software COMSOL and V_{DS} is the drain voltage. This way, the μ_{FE} as a

function of V_{GS} before and after the NP decoration can be determined.^[2,3] It is obvious that the peak μ_{FE} decreases from ≈ 3200 to ≈ 1900 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ after the surface decoration of CuO NPs, which might be attributed to the following reasons (Figure 1f). First of all, since CuO is an important p-type semiconductor and has a typical work function in the range of $\approx 5.2-5.4$ eV depending on the deposition conditions and crystallinity,^[22-24] which is higher than the one of intrinsically n-type InAs NWs (≈ 5.0 eV).^[25] In this case, when CuO NPs and InAs NWs are in contact, free electrons would transfer from the NW surface into the NPs; as a result, the free electron concentration of pristine InAs NWs is predicted semi-quantitatively to be decreased in half, yielding a depletion layer of ≈ 4.3 nm to surround the NW surface (see Table S1 in the Supporting Information for the details). This way, the effective NW channel width would get reduced by roughly 9 nm and the surface depletion would enhance the carrier scattering in lowering the μ_{FE} . A similar phenomenon of the surface depletion and mobility lowering was also observed in the previous work of tuning electronic transport properties of III-V NWFETs via metal cluster deposition.^[14] Second, when the InAs NW diameter is shrunk by ≈ 10 nm, the electron mobility is known to be reduced by 2 \times due to the combined effect of miniaturized effective NW channel and elevated carrier scattering from NW surface roughness.^[2,3] Based on these two factors, it is consistent to observe the decrease of μ_{FE} of InAs NWFETs after the CuO NP decoration.

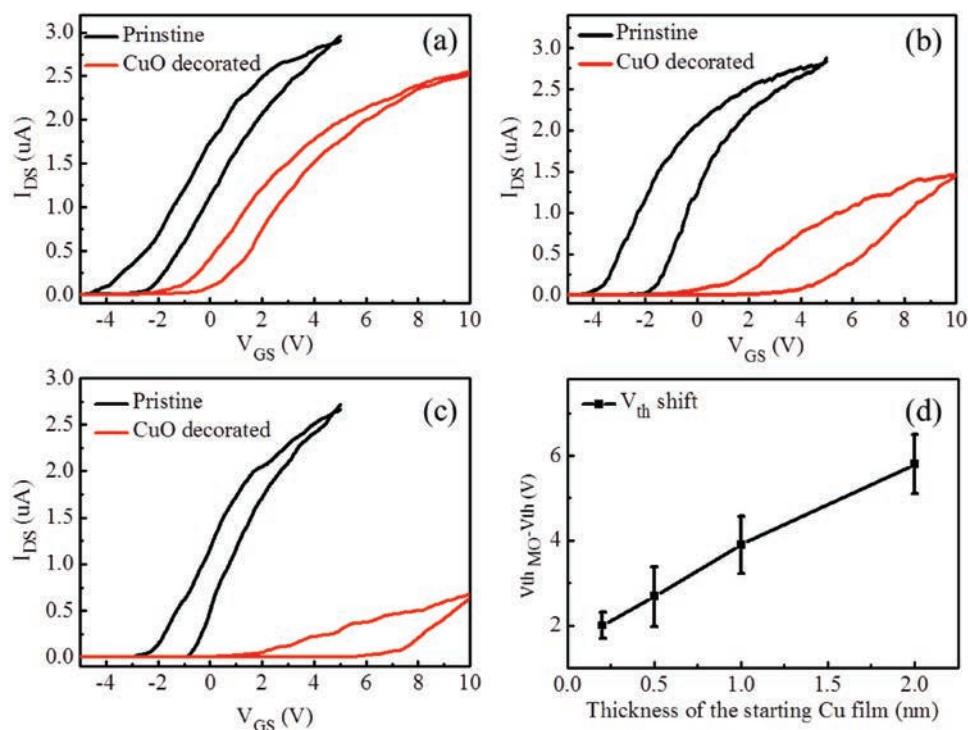


Figure 2. Effect of CuO NP surface decoration on electrical characteristics of InAs NWFETs with different NW channel thickness (V_{DS} of 0.1 V): a) 0.2 nm, b) 1.0 nm, c) 2.0 nm, and d) summary of V_{TH} shift as function of the starting Cu film thickness (10 individual devices are evaluated for the average in every sample group). CuO NPs are fabricated with pure Cu thin films with the thicknesses ranging from 0.2 to 2.0 nm, followed by annealing at 120 °C for 20 min in ambient. The V_{th} shift variation is come from the NW to NW variation existed in the NW synthesis.

At the same time, in order to assess and verify the modulation effect of CuO NP surface decoration on electrical properties of InAs NWs with different diameters, electrical characteristics of NW devices with different channel widths are thoroughly investigated. For instance, while the size of CuO NPs is maintained the same as ≈ 5 nm for the decoration, the thin device channel (i.e., $d \approx 20$ nm) exhibits the strongest V_{TH} shift of ≈ 4.5 V, as compared with the ones of medium channel (i.e., $d \approx 30$ nm) and thick channel (i.e., $d \approx 40$ nm) of ≈ 3.3 and ≈ 2.2 V, respectively (Figure S2, Supporting Information). All these observations are consistent to the fact that when the NW diameters becomes thicker, the corresponding surface-area-to-volume ratio would get decreased in weakening their surface carrier depletion induced by NP decoration and subsequently degrading their V_{TH} modulation effect. Furthermore, the influence of CuO NPs with different dimensions is also evaluated and confirmed for the decoration. In particular, with the purpose of minimizing any variation caused by different individual NWs, InAs NWFETs with the NW diameter of about 30 nm are selected and the effect of V_{TH} changes induced by various NP sizes is examined in a statistical manner based on the average of at least 10 devices. As shown in **Figure 2**, when the starting Cu film thickness is increased from 0.2 to 2.0 nm for the CuO NP surface decoration, the resulting magnitude of V_{TH} shift is observed to enlarge drastically from ≈ 2.0 to ≈ 5.8 V, but it also accompanies with the substantial μ_{FE} reduction to only ≈ 900 $cm^2 V^{-1} s^{-1}$ (Figure S3, Supporting Information). As soon as the NP size is further increased, the NPs would become too large and starts to aggregate forming a continuous network

deteriorating the intrinsic electronic transport properties of NWs (data not shown). On the other hand, as the initial Cu film goes thinner (e.g., < 0.5 nm), the obtained V_{TH} modulation effect is not sufficient to transform the NW device from D-mode into E-mode operation. Therefore, the optimal Cu film thickness is concluded to be 0.5 nm for the effective V_{TH} manipulation of typical high-performance InAs NWs ($d \approx 30$ nm), in which all these present important advancements to achieve energy-efficient E-mode NW devices via NP surface decoration without any significant degradation in their electron mobility for practical transistor applications.

To shed light on the fundamental influence of other semiconductor metal-oxide NPs with a various range of work functions on this surface decoration technique, electrical properties of InAs NWFETs surface decorated with NiO_2 , Ag_2O , and SnO_2 NPs are systematically investigated. In order to conduct a consistent comparison, the metal-oxide NPs are all fabricated from Ni, Ag, and Sn metal thin films with the nominal thickness of 0.5 nm, respectively, with the same processing conditions as the CuO NPs discussed above. It is as well noted that the chemical composition of decorated NiO_2 , Ag_2O , and SnO_2 NPs are all confirmed with XPS (Figure S4, Supporting Information). Similarly, the effect of surface decoration on InAs NWFETs is assessed separately for each metal-oxide NP based on at least 10 devices with the NW diameter of ≈ 30 nm to eliminate the variation induced by different individual NWs (**Figure 3**). Since both NiO_2 and Ag_2O NPs are typical p-type semiconductors with the higher work functions (i.e., ≈ 5.0 – 5.2 eV for NiO_2 and ≈ 5.0 – 5.3 eV for Ag_2O) than InAs NWs,^[26–29] they are anticipated

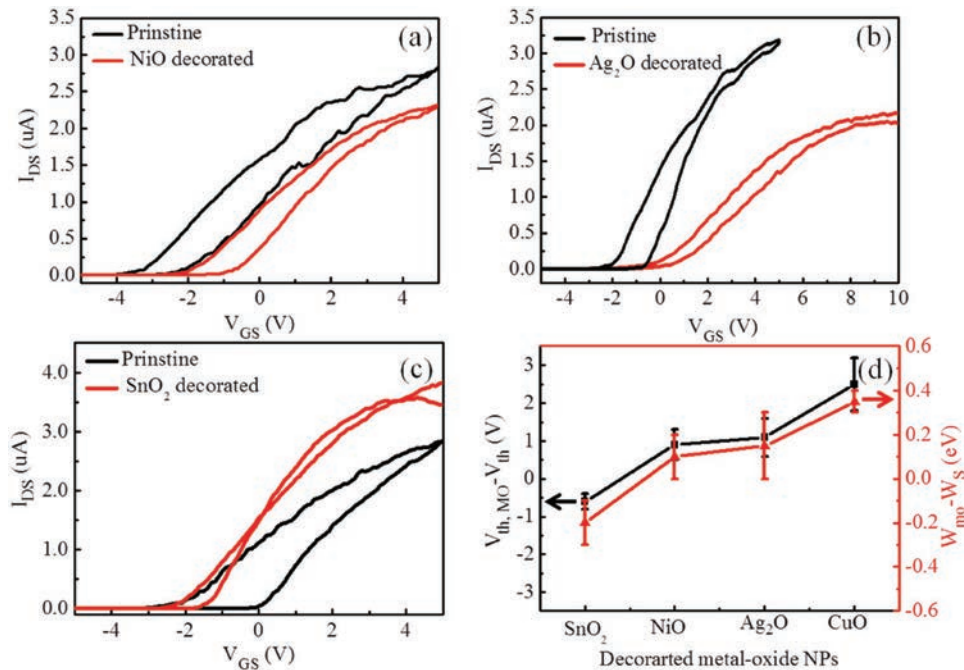


Figure 3. Effect of other metal-oxide NP surface decoration on electrical characteristics of InAs NWFETs (V_{DS} of 0.1 V): a) NiO, b) Ag_2O , c) SnO_2 , and d) summary of the V_{TH} shift as a function of the work function difference between the metal-oxide NPs decorated and InAs NWs (10 individual devices are evaluated for the average in every sample group). Metal-oxide NPs are prepared by depositing different pure metal films with a nominal thickness of 0.5 nm, followed by annealing at 120 °C for 20 min in ambient. The V_{th} shift variation is come from the NW to NW variation existed in the NW synthesis.

to alter the device V_{TH} toward the positive direction, contributing the average V_{TH} shift of 0.9 and 1.1 V, accordingly, for the E-mode operation (Figure 3a,b). Based on the semi-quantitative analysis, roughly 10% and 30% of free electrons are transferred from InAs NWs onto the NiO_2 and Ag_2O NPs for the formation of surface depletion layer; as a result, the μ_{FE} of NiO_2 and Ag_2O decorated InAs NWFETs would get decreased from ≈ 3000 to 2600 and 2000 $cm^2 V^{-1} s^{-1}$, respectively (Figure S5 and Table S1, Supporting Information). In contrast, as SnO_2 is an intrinsic n-type semiconductor and has a work function in the range of $\approx 4.7\text{--}4.9$ eV,^[30,31] which is lower than the one of InAs NWs. In this case, free electrons would be donated from SnO_2 NPs into InAs NWs once they are in contact. The device ON current is increased and the device V_{TH} is moved to the negative direction with an average shift of ≈ 0.8 V for D-mode operation (Figure 3c; Figure S5, Supporting Information). Interestingly, the corresponding μ_{FE} is slightly enhanced from 3000 to 3600 $cm^2 V^{-1} s^{-1}$ after the SnO_2 NP decoration. This mobility improvement can be attributed to the increased free electron concentration, roughly estimated as $\approx 1.6\times$ in Table S1 (Supporting Information), which participates in filling the potential barriers for the mobility enhancement.^[32,33] In brief, these semiconductor metal-oxide NPs can be simply applied to surface decorate the device channel of InAs NWs in order to effectively modulate the corresponding V_{TH} . The modulation effect is highly depended on the work function difference between the metal-oxide and NW materials ($W_{MO} - W_S$) such that metal-oxide NPs with the higher work function than NWs can lead to the V_{TH} shift toward the positive region, achieving E-mode device characteristics. While metal-oxide NPs with the lower work functions than NWs can move the V_{TH} to the negative

region for D-mode device operation. The larger $W_{MO} - W_S$ would give the greater magnitude in the V_{TH} shift. Notably, after the surface decoration, all NW devices exhibit the stable electrical characteristics when they are exposed to the ambient environment without any passivation for 500 h, which evidently indicates the remarkable inertness of these metal-oxide NPs and great potency of this decoration scheme for device fabrication.

Apart from the InAs NWs, this metal-oxide NP surface decoration approach can also be worked well on other III–V NW material systems, such as binary InP and ternary $In_{0.7}Ga_{0.3}As$. Employing the CuO NPs, fabricating with 0.5 nm thick of Cu films, the large device V_{TH} shift of ≈ 4.2 and ≈ 2.8 V toward the positive direction are observed for InP and $In_{0.7}Ga_{0.3}As$ NWFETs, respectively (Figures S6 and S7, Supporting Information). It is obvious that the positive work function difference between CuO NPs and InP NWs as well as CuO NPs and $In_{0.7}Ga_{0.3}As$ NWs would tend to move the device V_{TH} to the positive region achieving E-mode operation without any significant change in μ_{FE} . These are consistent with the results of InAs NWs, even though InP, $In_{0.7}Ga_{0.3}As$, and InAs have different work functions and other physical properties.^[14] All these would illustrate that the V_{TH} and device operation of typical III–V NWFETs can be controllably tailored by this simple metal-oxide surface decoration scheme with minimal changes in the electrical properties such as the ON current and μ_{FE} .

In an effort to further understand the physical mechanism of manipulating NW device characteristics via this metal-oxide NP surface decoration, the energy band diagrams of InAs NW decorated with various metal-oxide NPs, with dissimilar work functions, at different gate biases are demonstrated in Figure 4.

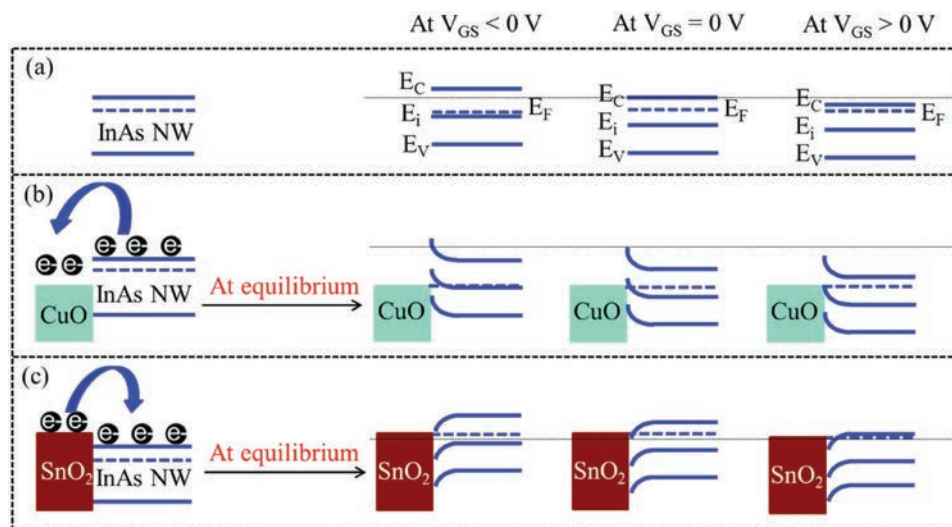


Figure 4. Schematic outlines of V_{TH} shift mechanisms of InAs NWFETs surface decorated with various metal-oxide NPs and the corresponding energy band diagram at different gate voltages: a) pristine InAs channel. b) Decorated with high work function CuO NPs to positively shift the device V_{TH} by withdrawing electrons from InAs NWs. c) Decorated with low work function SnO_2 NPs to negatively shift the device V_{TH} by donating electrons into InAs NWs.

For the as-prepared InAs NWs, the existing surface/interface defects are known to induce a relatively high electron concentration, which gives rise to pin the Fermi level (E_F) near or slightly above the conduction band edge at equilibrium ($V_{GS} = 0$ V) such that the NWs exhibit intrinsically n-type conductivity (Figure 4a).^[13,14,16,17] Thus, a negative gate voltage is necessary to push the E_F down or the conduction band up to deplete the excess free carriers achieving the device OFF state, in which the device is then performed in D-mode operation. When CuO NPs are surface decorated onto the device channel, owing to the positive $W_{MO} - W_S$,^[22–25] free electrons would flow from the InAs NWs onto CuO NPs and move the E_F down to the intrinsic level ($V_{GS} = 0$ V). This way, the equilibrium band diagram of InAs would be locally disturbed to bring an upward band-bending at the CuO NP/InAs NW interface, ultimately resulting in a positive V_{TH} shift. Because of this, the current at the zero gate voltage would be drastically reduced to almost zero unless a positive gate voltage is applied to move the conduction bands down, inducing a large current by extracting the free carriers, which is known as E-mode operation (Figure 4b). Alternatively, when SnO_2 NPs are decorated onto the InAs NW channel, the negative $W_{MO} - W_S$ would cause the band bending downward at the SnO_2 NP/InAs NW interface and move the E_F up to the conduction band. Then, free electrons would transfer from the NPs into the NWs, which results in the V_{TH} shift toward negative direction, higher ON current and μ_{FE} (Figure 4c). All these have further validated that the NW device V_{TH} and operation mode can be effectively modulated by this simple metal-oxide surface decoration. Since this band model is only qualitatively, more thorough and theoretical models are essential to further quantify the influence here.

Besides, instead of single NW devices, E-mode InAs NW-paralleled-arrayed FETs decorated with CuO NPs are also fabricated via NW contact printing in order to demonstrate the versatility of this metal-oxide surface decoration scheme for large-scale device integration for thin-film transistor (TFT) applications.^[7]

Specifically, the schematic view and scanning electron microscope (SEM) image of a representative global back-gated device surface decorated with CuO NPs in the channel are shown in Figure 5a,b. The NW filmed device has a print density of ≈ 2 NW μm^{-1} , a device width of ≈ 50 μm , and a channel length of 3.4 μm , accounting for a total of 95 NWs in the channel. Similar to single NW devices, the printed pristine NW filmed FET is initially operated in D-mode (Figure 5c). After CuO NPs are deposited onto the device channel with the same starting Cu film thickness of 0.5 nm, the V_{TH} is observed to shift to the positive direction to achieve the E-mode transistor. Although the μ_{FE} of this E-mode NW filmed device is reduced by half, attributing to the thinning of effective NW channel width due to the surface depletion layer upon contacting with CuO NPs, this reduced mobility of ≈ 1000 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ is still superior to the state-of-the-art metal-oxide, amorphous and polycrystalline Si TFTs.^[34–37] More importantly, the device performance of these NW filmed FETs can be further improved by shortening the channel length, optimizing the NW density and applying a top-gated structure with high-k dielectrics.

For practical utilizations, employing the aforementioned CuO NPs decorated E-mode InAs NW-paralleled-arrayed FET as the driver and another pristine D-mode InAs NW-paralleled-arrayed FET as the load with the source/drain terminals connected, a simple n-channel metal-oxide-semiconductor (NMOS) inverter can be integrated. The corresponding equivalent circuit diagram is given in the figure inset,^[14] while voltage transformation characteristics of the inverter are depicted in Figure 5e. It is clear that the inverter can efficiently alter the logic “1” (i.e., high input voltage) into the logic “0” (i.e., low output voltage) and vice versa. It is also worth noting that the inverter can function at a relative low voltage of ≈ 2 V and the input signal is upturned with a decent gain of ≈ 3.7 , along with the insignificant leakage current and reduced power consumption.^[38] In addition, the transient response to the alternating input voltage is as well investigated and impressively, the inverter can

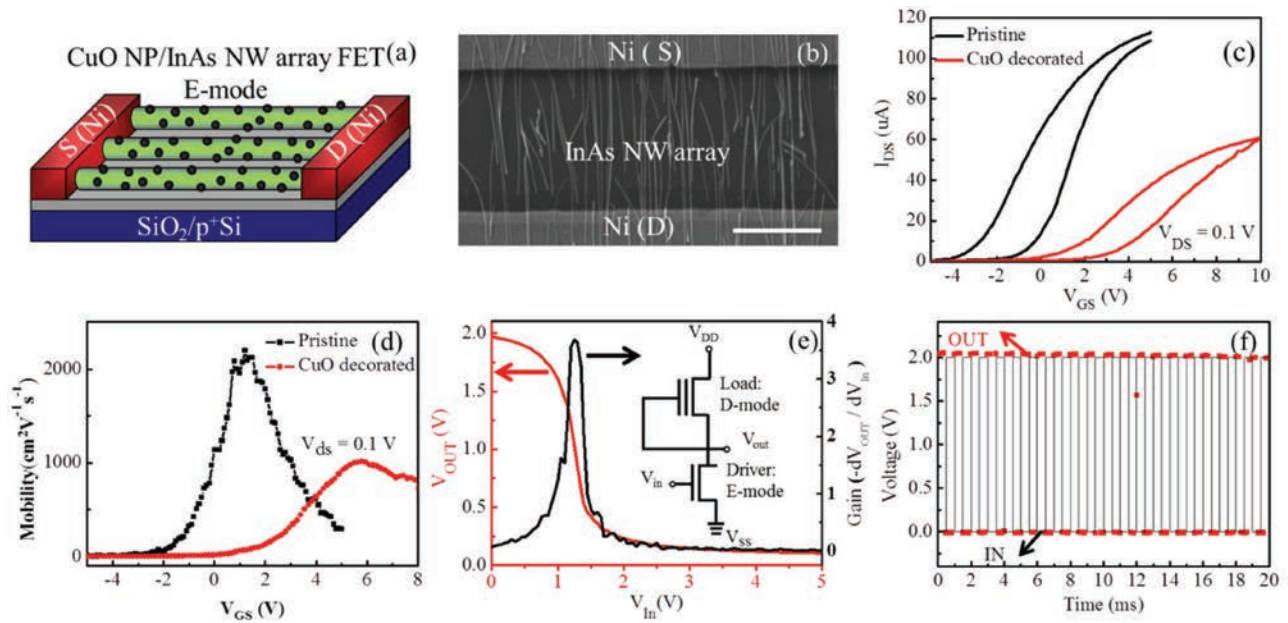


Figure 5. Practical application of metal-oxide NP surface decoration in achieving E-mode InAs NW filmed devices and in fabricating NMOS inverters. a) Schematic view of a E-mode InAs NW filmed device surface decorated with CuO NPs. b) Top view SEM image (scale bar = 2 μm) of a representative E-mode InAs NW filmed device. c) $I_{\text{DS}}-V_{\text{GS}}$ curves at $V_{\text{DS}} = 0.1$ V for the InAs NW filmed device with and without the CuO NP decoration. d) The corresponding field-effect electron mobility as a function of the gate voltage. e) The voltage transfer characteristics (red line) and the corresponding gain (black line) of the representative NMOS inverter, the inset is the schematic of equivalent circuit diagram of the inverter. f) The output signal of the NW array inverter at 1000 Hz 2 V square waveform, demonstrating a fast response of the inverter. CuO NPs are prepared from the pure Cu film with nominal thickness of 0.5 nm, followed by annealing at 120 $^{\circ}\text{C}$ for 20 min in ambient.

be worked proficiently with a 1000 Hz and 2 V square waveform input. As a result, the NMOS inverter consisted of n-type E-mode and D-mode InAs NW-paralleled-arrayed FETs can be operated effectively at both steady and transient conditions, illustrating that a reliable and versatile metal-oxide NP decoration scheme can be applied to modulate the V_{TH} and control the operation mode of InAs NW-paralleled-arrayed FETs for circuit integration. All of these results have clearly revealed the potential of realizing large-scale NW devices as fundamental building blocks for future electronics.

3. Conclusion

In summary, a simple and reliable metal-oxide NP surface decoration scheme has been developed to manipulate the device performance of III-V NWFETs, which can effectively adjust the device V_{TH} with minimal changes in their device characteristics by simply tuning the $W_{\text{MO}} - W_{\text{S}}$. Since CuO NPs have the higher work function than the ones of most III-V NWs, the decorated NPs would shift the device V_{TH} to positive direction to achieve E-mode behavior. On the other hand, the SnO_2 NPs, which have the relatively much lower work function, would move the V_{TH} toward negative voltage to exhibit D-mode operation. In addition, high-performance E-mode InAs NW-paralleled-arrayed devices have also been successfully fabricated with the channel surface decorated with CuO NPs, which indicate the practicability of this metal-oxide NP decoration approach to the large-scale device processing. More importantly, NMOS inverters, utilizing conventional D-mode and metal-oxide NPs

decorated E-mode InAs NW thin filmed FETs, are as well fabricated to demonstrate the reliable control of device V_{TH} for circuit integration. All these findings reveal explicitly the bright prospects of the metal-oxide NP surface decoration scheme for next-generation large-scale, high-performance, low-power nanoelectronic devices and circuits.

4. Experimental Section

NW Synthesis: InAs, InP, and $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ NWs studied in this work were prepared by a solid-source catalytic chemical vapor deposition method in a dual-zone horizontal tube furnace as previously reported.^[2,4,39,40] Briefly, the solid source powders (1 g, 99.995% purity) were heated in the upstream zone of the furnace, while the growth substrate (Si with 50 nm thermally oxide on top) was covered with the Au or Ni catalyst film deposited with thermal evaporation with a nominal thickness of 0.5 nm, and placed in the middle of the downstream zone with a tilt angle of $\approx 20^{\circ}$ as well as a distance of 10 cm away from the source. The evaporated precursors were then transported to the downstream zone by high purity H_2 carrier gas (100 sccm, 1 Torr) for the synthesis of NWs. The entire duration of the growth cycle was 30 min.

FET Fabrication and Characterization: After the growth, NWs were harvested in anhydrous ethanol by sonication, and then drop-casted onto holey-carbon-film-coated copper grids for transmission electron microscopy (TEM; JEOL 2100F), onto intrinsic Si for XPS (Thermo Scientific, ESCALAB 250), and onto Si/SiO₂ substrates (50 nm thermal oxide on heavily doped Si) for the fabrication of back-gated FETs. These NWFETs were fabricated using a standard UV lithography process, followed by the thermal deposition of Ni (50 nm) film and metal lift-off. Notably, a 5 s HF (1%) etch was applied immediately prior to the Ni deposition to remove the native oxide on the exposed NW surface in order to ensure the ohmic contact formation. Next, after the device

fabrication, semiconductor metal-oxide NPs (i.e., CuO, Ag₂O, NiO, or SnO₂) could be surface decorated onto the FET channels by thermally depositing metal thin films (i.e., Cu, Ag, Ni, or Sn) and subsequent thermal annealing at 120 °C for 20 min to completely transform metal NPs into metal-oxide formats.^[30] After that, electrical properties of the finished devices were investigated with a cryogenic probe station (Janis ST-500) and a semiconductor parameter analyzer (Agilent 4155C) at room temperature.

Typical SEM images of single NWFETs and NW-paralleled-arrayed FETs were taken by SEM (Philips XL30). Bright-field TEM (Philips CM-20) was performed to survey the morphology of metal-oxide NPs decorated onto the NWs. Chemical compositions of the deposited metal-oxide NPs after annealing were characterized by XPS.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This research was financially supported by the National Natural Science Foundation of China (51402160, 51672229, and 61504151), the Natural Science Foundation of Shandong Province, China (ZR2014EMQ011), the General Research Fund (CityU 11204614), and the Theme-based Research Scheme (T42-103/16-N) of the Research Grants Council of Hong Kong SAR, China, the Science Technology and Innovation Committee of Shenzhen Municipality (Grant JCYJ20160229165240684), and Taishan Scholar Program of Shandong Province, China.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

enhancement modes, III–V nanowires, metal-oxide nanoparticles, surface decoration, threshold voltage

Received: March 1, 2017
Revised: March 31, 2017
Published online: May 8, 2017

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