Controlled Growth of Heterostructured Ga/GaAs Nanowires with Sharp Schottky Barrier

Zhou Wang,[†,‡] Ying Wang,[†,§] Xinyuan Zhou,[†] Zaixing Yang,[∥] Yanxue Yin,[∥] Jie Zhang,[‡] Ning Han,*[,†,§] Johnny C. Ho,*[,⊥] and Yunfa Chen[†,§]

[†]State Key Laboratory of Multiphase Complex Systems, Institute of Process Engineering, Chinese Academy of Sciences, Beijing 100190, P. R. China

[‡]State Key Laboratory of Chemical Resource Engineering, Beijing University of Chemical Technology, Beijing 100029, P. R. China

[§]Center for Excellence in Regional Atmospheric Environment, Institute of Urban Environment, Chinese Academy of Sciences, Xiamen 361021, P. R. China

[∥]Center of Nanoelectronics and School of Microelectronics, Shandong University, Jinan 250100, P. R. China

[⊥]Department of Materials Science and Engineering, City University of Hong Kong, Hong Kong SAR, P. R. China

S *Supporting Information*

ABSTRACT: Because of the inevitable Fermi level pinning on surface/interface states of nanowires, achieving high-performance nanowire devices with controllable nanoscale contacts is always challenging but important. Herein, single-crystalline heterostructured Ga/GaAs nanowires with sharp hetero-Schottky interfaces have been successfully synthesized on amorphous substrates by utilizing Au nanoparticles as catalytic seeds via chemical vapor deposition. These nano-wires are found to grow with the hemispherical Au_7Ga_2 catalytic tips following the vapor−liquid−solid mechanism. During the growth, simply by manipulating the source and growth temperatures, the Ga precipitation rate from Au−Ga

alloy tips as well as the reaction rate of Ga precipitates with As can be reliably controlled in order to tailor the length (0−170 nm) of Ga nanowire segments obtained in the heterostructure. When configured into field-effect transistors, these Ga/GaAs NWs exhibit the p-type conductivity with a sharp hetero-Schottky barrier of ∼1.0 eV at the atomically connected Ga segment/GaAs NW body interface, in which this barrier height is close to the theoretical difference between the GaAs Fermi level (5.1−5.3 eV) and the Ga work function (∼4.3 eV), suggesting the effective formation of nanoscale contact by minimizing the Fermi level pinning, being advantageous for advanced nanoelectronics.
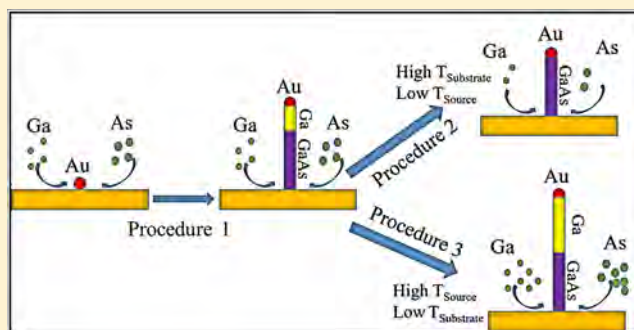
1. INTRODUCTION

Because of their appropriate direct band gaps and remarkably high carrier mobilities, III−V compound semiconductor nanowires (NWs), such as gallium arsenide (GaAs) and indium arsenide (InAs), are widely investigated for various applications in next-generation electronics, optoelectronics, and others.[1−8] In particular, both intrinsic and axially or laterally p/n doped NWs are successfully synthesized by the catalytic vapor−liquid−solid (VLS) and/or vapor−solid−solid (VSS) mechanisms utilizing molecular beam epitaxy (MBE),[9−11] metal−organic chemical vapor deposition (MOCVD),[11−13] laser ablation, etc.[14] However, since these NW materials have the relatively large surface-to-volume ratio with a significant amount of surface dangling bonds, all these unsaturated bonds would contribute a substantial amount of surface states, inducing the serious surface Fermi level pinning.[15−18] Inevitably, when configured into NW devices, this pinning would make the contact barrier between NWs and metals being independent of the metal work function;

therefore, special attention is required for the metallization of these NWs.[19,20] For example, InAs NWs typically have their surface Fermi level pinned in the conduction band, yielding a great challenge to achieve efficient contacts to their p-type NWs, which necessitates a surface InP remote doping strategy there.[21,22] As a result, it is technologically difficult to investigate and implement the effective nanoscale contact with III−V semiconductor NWs.

On the other hand, during the NW synthesis, the metal catalyst, such as the commonly adopted Au nanoparticle (NP), would atomically contact the NW body without any surface/interface state.[23] For instance, Tambe et al. have previously reported the Schottky barrier between Au catalyst and GaAs NW body of being ∼0.6 eV, which is similar to the one obtained from theoretical calculations, suggesting that there is

not any significant surface Fermi level pinning.[24] Later, in our experiments, we also observed a high open circuit voltage of ∼0.6 V for GaAs NW solar cells based on the Schottky barrier between Au catalyst and GaAs NW body, while a very low voltage (e.g., 0.1 V) was witnessed when thermally deposited Au electrode was substituted for the Au catalyst as electrical contacts. All these results have clearly highlighted the significant difference between the atomically contacted metal with GaAs NWs and the thermally deposited metal onto GaAs NWs.[22] Nevertheless, as the GaAs NW growth is highly selective to the choice of metal catalysts, it is hence problematic to explore the efficient contact of GaAs NWs with other metals expect for the commonly adopted Au catalyst.

In this work, by precisely manipulating the CVD condition with Au NPs as catalysts, we have successfully achieved the controllable growth of heterostructured Ga/GaAs NWs with the sharp hetero-Schottky interface.[25−27] Specifically, the hemispherical single-crystalline Au_7Ga_2 catalytic tips are clearly observed, which infers the growth of Ga−GaAs NWs following the VLS mechanism. Moreover, there is not any noticeable amount of defects along the entire length of NWs (>10 μm) with the average NW diameter of 23.5 ± 6 nm. Importantly, based on the careful electrical measurement, a sharp Schottky barrier of ∼1.0 eV is established between Ga and GaAs segments, which is perfectly consistent with the theoretical barrier (i.e., work function difference between Ga and GaAs, 5.3 − 4.3 = 1.0 eV). All these findings evidently demonstrate the effective control of heterostructured Ga−GaAs NW growth with the sharp Schottky interface, being advantageous for many Schottky junction devices and their applications.[28,29]

2. EXPERIMENTAL SECTION

Figure 1 depicts the schematic illustration of the experimental setup and the growth procedure of GaAs NWs studied here. In detail, a two-
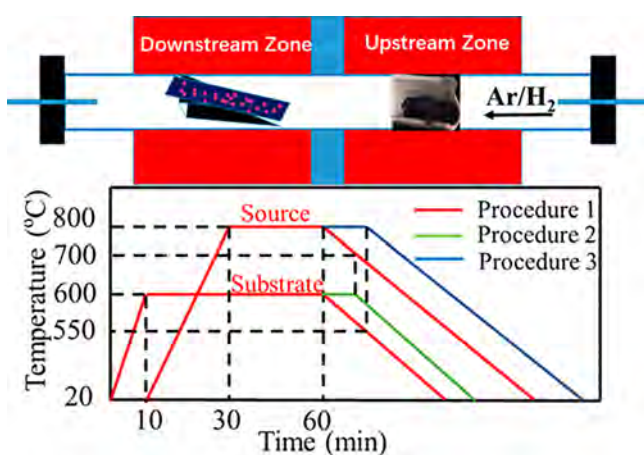

Figure 1. Schematic illustration of the dual-zone horizontal tube furnace and the experimental procedures for the GaAs NW growth.

temperature zone tube furnace was adopted as the reactor, with one end for the solid source placement (upstream) and the other end for the NW growth (downstream). Prior to the CVD synthesis, (100)-oriented Si/SiO_2 (50 nm thick thermally grown oxide) substrates were cleaned with ultrasonic bath in deionized water, ethanol, and acetone, accordingly, followed by the nitrogen blow dry. After that, the as-prepared Au NPs[30] (∼11 nm in the diameter with the corresponding TEM image, size distribution, and synthesis method shown in the Supporting Information, Figure S1) were evenly

dispersed on top of the substrates. The high purity GaAs powder (0.5 g, 99.95%) then served as the Ga and As precursor sources, which was placed in an alumina crucible and positioned in the middle of the upstream zone. During the growth, the prepared substrate was placed at the center of the downstream zone with a tilt angle of 20°. H_2 (5% in Ar) was used as the carrier gas to transport the thermally vaporized GaAs, while the process pressure was maintained at 5.0 Torr for the entire duration of the process (i.e., 30 min). Eventually, the heating of the source and substrate was stopped according to procedures 1−3 listed in Figure 1 with the natural cooldown to room temperature under the H_2 (5% in Ar) flow. Under this condition, the grown NWs were chemically intrinsic without any intentional dopants.

Furthermore, the crystallinity of grown GaAs NWs was investigated by employing an X-ray diffractometer with Cu Kα radiation (1.5406 Å) operated at 40 kV and 40 mA in the diffraction angle (2θ) from 20° to 60°. Their morphologies were also characterized by a scanning electron microscope (SEM). High-resolution transmission electron microscopy (HRTEM) images and energy dispersive spectroscopy (EDS) of NWs were obtained on a JEOL JEM-2100F microscope with an accelerating voltage of 200 kV. For TEM and EDS studies, the GaAs NWs were first suspended in the anhydrous ethanol solution by ultrasonication and then drop-casted onto the Cu grid covered with carbon film for the corresponding characterization.[31]

On the other hand, the GaAs NW FET devices were as well prepared by dispersing the NWs (suspended in anhydrous ethanol) onto the precleaned p+ Si/SiO_2 substrates (50 nm). A series of cross marks and squares around the NWs were prepared by electron beam lithography (EBL) to precisely determine their patterning location in the subsequent process as shown in Figure S2. Next, regions for source and drain electrodes were patterned by EBL, while the Ni film of 60 nm was then deposited by e-beam evaporation followed by a lift-off process. The electrical performance of fabricated back-gated NW FETs was finally characterized with a standard electrical probe station (Lakeshore Cryotronics) and a Keithley 4200 semiconductor parameter analyzer.

3. RESULTS AND DISCUSSION

In the solid-source CVD system, the Ga precursor would first evaporate from the GaAs powder and then alloy with Au NPs to perform as the catalytic seeds. Then, the supersaturated Ga precursors are precipitated and reacted with the As precursor, resulting in the growth of GaAs NWs.[32,33] Following the growth procedure 1 (Figure 1), when the growth temperature and source temperature are fixed at 600 and 800 °C, respectively, the H_2 (5% in Ar) gas flow is controlled to 100 sccm (i.e., pressure ∼5.0 Torr), and the growth duration is maintained for 30 min, very dense, smooth, long (>10 μm) and uniform GaAs NWs are readily obtained as presented in the SEM and TEM images in Figures 2a,b. Based on the TEM images, the NW diameter distribution can be determined as 23.5 ± 6 nm from the statistics of 45 individual NWs as given in Figure 2c. The relatively larger diameter of NWs as compared with the one of Au colloids can be attributed to several aspects, such as the incorporation of Ga into Au, the shape changes of Au sphere into Au_7Ga_2 hemisphere, and the increased NW diameter by the Ostwald's ripening effect at high temperatures.[1] To further explore the crystallinity of obtained NWs, XRD is performed as shown in Figure 2d. Two dominant diffraction peaks are found at 2θ angles of 27.30° and 45.41° without considering the substrate peaks, where these two peaks are corresponded to the cubic zincblende (ZB) GaAs (111) and (220) planes.[34]

At the same time, HRTEM and EDS mapping are also performed on the obtained NWs as shown in Figure 3. Explicitly, a hemispherical Au-based catalytic seed is seen at the tip of the NW (Figure 3a), which implies the VLS growth
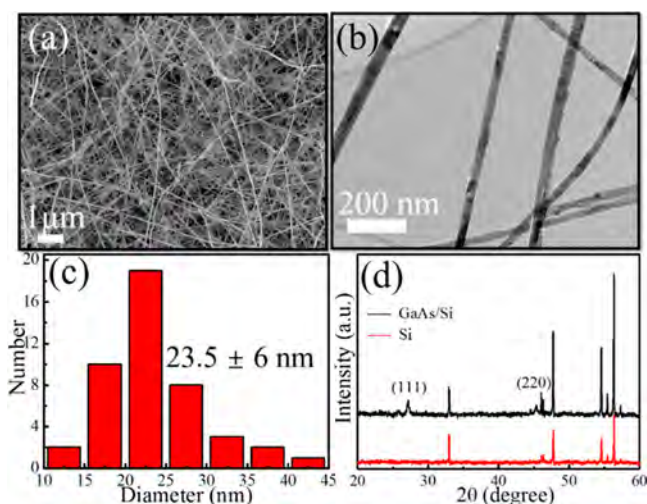
Figure 2. (a) SEM image of the GaAs NWs prepared by Au NPs as the catalysts (~11 nm in diameter) and growth procedure 1. (b) TEM image of the NWs. (c) Diameter statistics of 45 NWs observed in the TEM images. (d) XRD spectra of the NWs and the bare substrate.
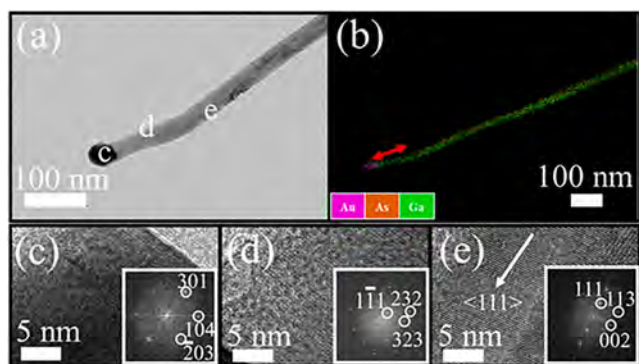

Figure 3. (a) TEM image of a typical GaAs NW prepared by the growth procedure 1. (b) Corresponding EDS mapping of the NW. (c) HRTEM image and FFT (inset) of the Au_7Ga_2 alloy tips. (d) HRTEM image and FFT (inset) of the Ga NW segment. (e) HRTEM image and FFT (inset) of the GaAs NW body.

mechanism of the GaAs NW. Interestingly, a Ga segment (45−50 nm in the length) is also observed between the Au catalyst tip and the GaAs NW body as identified by the EDS mapping (Figure 3b). In addition, the HRTEM and corresponding fast Fourier transformation (FFT) images of the Au−Ga catalyst, Ga segment and GaAs NW body not only illustrate the single-crystalline hexagonal Au_7Ga_2 catalyst tip and cubic ZB GaAs NW body along the ⟨111⟩ direction but also indicate the single-crystalline orthogonal Ga segment being in the good accordance with EDS mapping results. It is also noted that when the EDS line scan is taken along the NW in the axial direction, there is again a clear confirmation of the Ga segment existed between the Au−Ga catalyst tip and the GaAs NW body with sharp heterointerfaces of less than 10 nm in the junction depth (Figure 4). In the literature, it is reported that a short GaAs neck of 10−20 nm in the length could be formed between the Au−Ga catalyst and the GaAs NW body in chemical beam epitaxy simply by cooling the NWs in As atmosphere while switching off the Ga precursor. This way, the Ga extraction could be occurred from the Au−Ga alloy tip by the reaction with the excess As precursor. This Ga
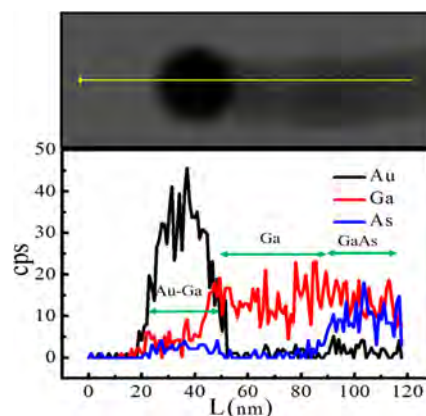

Figure 4. EDS line scan along a representative GaAs NW obtained by the growth procedure 1. The curves indicate the distribution of Au, Ga, and As elements along the axial direction of the NW.

consumption from the Au−Ga alloy would then make the catalyst tip become smaller, and thus the neck would be shrunk gradually.[12,35] However, until now, there is not any metallic Ga segment reported for the GaAs NW growth. The origin of this Ga segment is still uncertain, but we can presumably exclude its contribution from the Au−Ga alloy. It is because even if we realloyed the segment, it would turn into the larger Au−Ga alloy seed with a size of ~45 nm. Since the diameter of Au-catalyzed GaAs NWs is highly depended on the size of catalyst,[1,36] this larger seed of ~45 nm would subsequently lead to the growth of thicker NWs, which is in a distinct contrast to the ones (i.e., NWs with a diameter of ~25 nm) observed in this study. As a result, this Ga segment is not merely a cooling precipitation of Ga from the Au−Ga alloy.

To shed light on the formation mechanism of this Ga segment, many experimental parameters, such as the carrier gas flow rate, source powder dosage, source and substrate temperatures, etc., have been tailored in order to assess their effects on the Ga segment. It is found that the source and substrate temperatures are the key factors in regulating the growth of Ga segment. As shown in the temperature profile in Figure 1, when the growth is deviated from the typical condition (procedure 1) by lowering the source temperature from 800 to 700 °C after 30 min of growth, keeping the substrate temperature at the same growth temperature of 600 °C, and then turning off both zones together to cool to room temperature, it is defined as the growth procedure 2. Using this profile, the Ga segment is almost disappeared (<10 nm in length), and the process is converted into conventional GaAs NW growth as depicted in Figure 5. The alloy tip and GaAs NW body can be obviously observed from the TEM and EDS mapping (Figures 5a,b). The hexagonal Au_7Ga_2 alloy tip and cubic ZB NW body can also be confirmed based on the HRTEM image and corresponding FFT pattern (Figures 5c,d). On the other hand, when the growth procedure 3 is adopted, where the substrate temperature is first cooled from 600 to 550 °C after 30 min of growth while the source temperature is kept at 800 °C, and then both zones are switched off together to cool to room temperature, the Ga segment would become longer to the length of ~170 nm (Figures 6a,b). The crystalline phases of both Ga segment and GaAs NW body remained unchanged as shown in the HRTEM image and corresponding FFT pattern (Figures 6c,d). To evaluate the wire-to-wire variation, more than 10 NWs are characterized for each growth
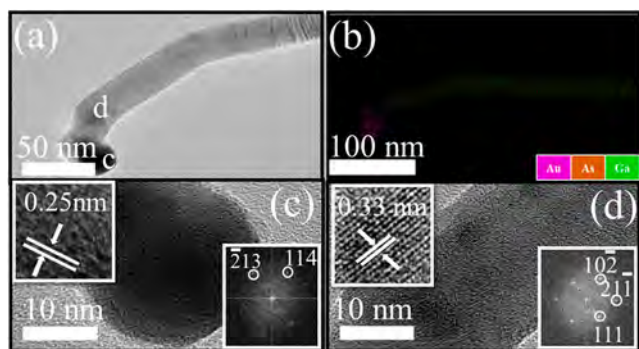
Figure 5. (a) TEM image of a typical GaAs NW prepared by the growth procedure 2. (b) Corresponding EDS mapping of the NW. (c) HRTEM image and FFT (inset) of the Au$_7$Ga$_2$ alloy tip. (d) HRTEM image and FFT (inset) of the GaAs NW body.
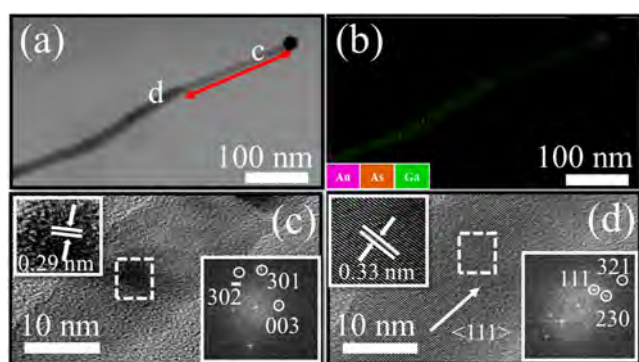

Figure 6. (a) TEM image of a typical GaAs NW prepared by the growth procedure 3. (b) Corresponding EDS mapping of the NW. (c) HRTEM image and FFT (inset) of the Ga segment. (d) HRTEM image and FFT (inset) of the GaAs NW body.

procedure with the length statistics of Ga segment as compiled in Figure 7. All these experimental results clearly confirm the
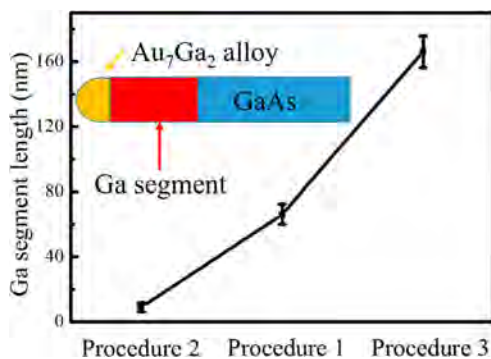

Figure 7. Average length and standard deviation of the Ga segment obtained under the three experimental NW growth procedures.

formation of heterostructured Ga/GaAs NWs with sharp heterointerfaces as well as the controllable Ga segment length by the manipulation of growth temperatures.

In the typical VLS growth of III−V NWs, when Au catalysts are utilized, the group III precursors are generally believed to be diffused and precipitated from the Au−III alloy and then reacted with the gas-phase group V precursor to yield the NW growth.[37] The reaction rate is usually far higher than the ones of diffusion and precipitation; hence, the group III precursor is

consumed totally without any literature report for the group III only NW segment. However, in this work, we can simply tailor the precursor concentration via changing the source temperature as well as modify the reaction rate via varying the substrate temperature; then the precipitation of group III species and the reaction of between group III and V components can be decoupled. In this case, when the relatively lower substrate temperature, such as 550 °C, is adopted together with the low As precursor concentration, the precipitation of Ga would become faster than the reaction of between Ga and As; therefore, the Ga segment is obtained. Notably, the sharp heterointerfaces can be formed here, which can be attributed to the precise and efficient control of temperatures in the CVD system. On the contrary, at the higher substrate temperature (e.g., 600 °C) with abundant As concentration, the Ga precipitate would be consumed much faster, leading to the diminishing of the Ga segment. In the meanwhile, the single crystalline Au$_7$Ga$_2$ catalyst alloy might also take part in the Ga diffusion and precipitation tuning, which requires further investigations. All these processes are also schematically illustrated in Figure 8, where a trade-off between the Ga precipitation and the reaction between Ga and As is clearly shown.
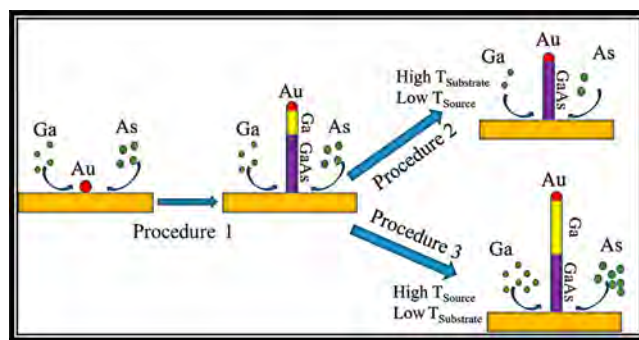

Figure 8. Schematic illustration of the growth process described for the novel heterostructured Ga/GaAs NWs with sharp heterointerfaces.

At the same time, it is also important to evaluate electrical properties of the Au-catalyzed heterostructured Ga/GaAs NWs. In this case, NW FETs were fabricated using Ni (~60 nm) source/drain (S/D) metal contacts configured in a global back-gated geometry. The 50 nm thick thermal oxide was employed as the gate dielectric while the degenerately boron-doped Si substrate was utilized as the back-gate.[38] The measured NWs were prepared with procedure 3, in which the Ga segment length is the longest with the length of ~160 nm. Figure 9a illustrates a representative device fabricated with an individual GaAs NW as the device channel with a diameter of ~20 nm and a channel length of ~600 nm. Notably, the Au−Ga alloy tip is also clearly seen beneath the source electrode.[39] As Ni electrode covers 90 nm of the Ga "neck" (<160 nm, Figure 9a, inset), it can be confirmed that the Ga/GaAs interface is left in the channel. The typical I−V curves are then shown in Figure 9b, where a diode like I−V curve with an onsite voltage of ~1 V is clearly shown. This Schottky barrier is mainly attributed to the atomically connected Ga/GaAs interface without any trap states and hence without any significant Fermi level pinning there, which is similar to the electrical contact characteristics of between Au−Ga alloy and GaAs NW reported in the past.[40] On one hand, Ni has a
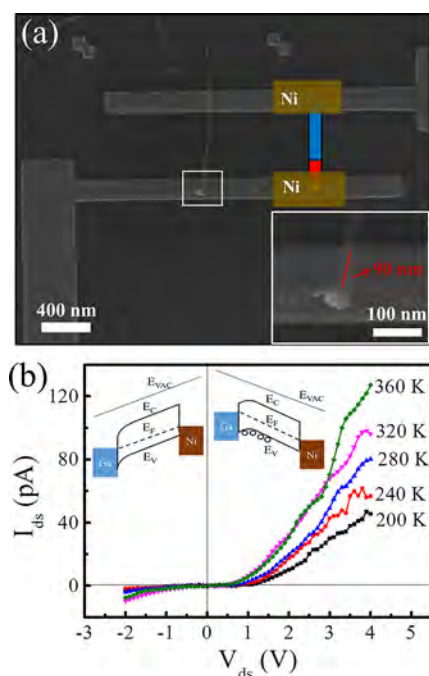
Figure 9. (a) SEM image of one typically measured EBL device. Inset: magnified SEM image of the area framed by the rectangle shows that Ni electrode covers the partial Ga "neck" (90 nm). Inset: schematic of the device fabricated by EBL. One Ni electrode covers the partial Ga "neck", and the other Ni electrode covers the GaAs NW. (b) Temperature-dependent $I-V$ curves of NW device at $V_{gs} = -10$ V.

relatively similar work function to the GaAs (5.1−5.3 eV, p-type as verified in Figure S3), and ohmic contact is therefore resulted therein.[41,42] This was further verified by the $I-V$ characteristics of the thermally deposited Ni electrodes on the GaAs NW without Ga segment, as typically shown in Figure S4. On the other hand, as Ga has the relatively lower work function (∼4.3 eV), a Schottky barrier of ∼1.0 eV (5.3 − 4.3 = 1.0) would be formed when Ga contacts with GaAs.[43]

The temperature-dependent $I-V$ measurements were also carried out in order to extract the Schottky barrier, φ_B, by the conventional thermionic electron emission model with the following analytical expression:

$$I_s = A^* T^2 \exp\left(-\frac{\varphi_B}{k_B T}\right) \qquad (1)$$

where I_s is the saturation current, A^* is the Richardson's constant, k_B is the Boltzmann constant, q is the charge of an electron, and T is the temperature. In this case, the Schottky barrier height can be extracted from the slope of the linear parts of the $\ln(I_s/T^2)$ versus $1000/T$ plot.[44,45] However, the saturation currents are too small to be precisely resolved in the range 100−360 K, making it impossible to plot the $\ln(I_s/T^2)$ versus $1000/T$ relationship. Despite this, we can still estimate the Schottky barrier by the onsite voltage of ∼1 V, which can also be observed by several other NW FET devices. Therefore, all these results show the controlled synthesis of the heterostructured Ga/GaAs NWs with intrinsic Schottky barrier of ∼1 eV, being promising for the contact design for next-generation nanowire nanoelectronics.

4. CONCLUSIONS

In summary, single crystalline heterostructured Ga/GaAs NWs have been successfully synthesized on noncrystalline SiO_2/Si substrates via the VLS mechanism with hemispherical Au_7Ga_2 catalytic tips by utilizing Au nanoparticles as the starting catalyst. Specifically, the Ga NW segment length can be reliably tailored by manipulating the GaAs source evaporation and NW growth temperature. This implies that the origin of these Ga segments mostly comes from the trade-off between the Ga diffusion/precipitation from Au−Ga alloy tips as well as the reaction of precipitated Ga with As. Importantly, these Ga/GaAs NWs exhibit a sharp hetero-Schottky barrier of ∼1.0 eV at the interface between atomically connected Ga and GaAs, in which this high quality interface would make the barrier independent of the commonly observed surface Fermi level pinning effect. All these results evidently illustrate the promise of this heterostructure control of GaAs NWs and their potential applications for various Schottky devices.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.cgd.8b00409.

TEM and diameter distribution of Au nanoparticle catalysts, EBL marks, $I-V$ curves of Ga/GaAs NWs with the hetero-Schottky barrier, and $I-V$ curves of GaAs NWs without Schottky barrier (PDF)

■ AUTHOR INFORMATION

Corresponding Authors
*(N.H.) E-mail: nhan@ipe.ac.cn.
*(J.C.H.) E-mail: johnnyho@cityu.edu.hk.
ORCID Ⓓ
Jie Zhang: 0000-0002-3059-1978
Ning Han: 0000-0001-9177-6792
Johnny C. Ho: 0000-0003-3000-8794
Author Contributions
Z.W. and Y.W. contributed equally to this work.
Notes
The authors declare no competing financial interest.

■ REFERENCES

(1) Han, N.; Wang, F.; Hou, J. J.; Yip, S. P.; Lin, H.; Fang, M.; Xiu, F.; Shi, X.; Hung, T. F.; Ho, J. C. Manipulated Growth of GaAs Nanowires: Controllable Crystal Quality and Growth Orientations Via a Supersaturation-Controlled Engineering Process. *Cryst. Growth Des.* **2012**, *12*, 6243−6249.

(2) Gudiksen, M. S.; Lauhon, L. J.; Wang, J.; Smith, D. C.; Lieber, C. M. Growth of Nanowire Superlattice Structures for Nanoscale Photonics and Electronics. *Nature* **2002**, *415*, 617−620.

(3) Pauzauskie, P. J.; Yang, P. Nanowire Photonics. *Mater. Today* **2006**, *9*, 36−45.

(4) Yoon, J.; Jo, S.; Chun, I. S.; Jung, I.; Kim, H. S.; Meitl, M.; Menard, E.; Li, X.; Coleman, J. J.; Paik, U.; Rogers, J. A. GaAs Photovoltaics and Optoelectronics Using Releasable Multilayer Epitaxial Assemblies. *Nature* **2010**, *465*, 329−333.

(5) Sun, Y.; Rogers, J. A. Fabricating Semiconductor Nano/Microwires and Transfer Printing Ordered Arrays of Them onto Plastic Substrates. *Nano Lett.* **2004**, *4*, 1953−1959.

(6) Rafique, S.; Han, L.; Zhao, H. Chemical Vapor Deposition of M-Plane and C-Plane InN Nanowires on Si (100) Substrate. *J. Cryst. Growth* **2015**, *415*, 78−83.

(7) Glaser, M.; Kitzler, A.; Johannes, S.; Prucnal, S.; Potts, H.; et al. Synthesis, Morphological, and Electro-Optical Characterizations of Metal/Semiconductor Nanowire Heterostructures. *Nano Lett.* **2016**, *16*, 3507−3513.

(8) Dhaka, V.; Haggren, T.; Jussila, H.; Jiang, H.; Kauppinen, E.; Huhtio, T.; Sopanen, M.; Lipsanen, H. High Quality GaAs Nanowires Grown on Glass Substrates. *Nano Lett.* **2012**, *12*, 1912−1918.

(9) Colombo, C.; Spirkoska, D.; Frimmer, M.; Abstreiter, G.; Morral, A. F. I. Ga-Assisted Catalyst-Free Growth Mechanism of GaAs Nanowires by Molecular Beam Epitaxy. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2008**, *77*, 761−768.

(10) Ramdani, M. R.; Gil, E.; Leroux, Ch.; André, Y.; Trassoudaine, A.; Castelluci, D.; Bideux, L.; Monier, G.; Robertgoumet, C.; Kupka, R. Fast Growth Synthesis of GaAs Nanowires with Exceptional Length. *Nano Lett.* **2010**, *10*, 1836−1841.

(11) Cifuentes, N.; Limborco, H.; Viana, E. R.; Roa, D. B.; Abelenda, A.; da Silva, M. I. N.; Moreira, M. V. B.; Ribeiro, G. M.; de Oliveira, A. G.; Gonzalez, J. C. Electronic Transport in P-Type Mg-Doped GaAs Nanowires. *Phys. Status Solidi B* **2016**, *253*, 1960−1964.

(12) Larsson, M. W.; Persson, A. I.; Wallenberg, L. R.; Samuelson, L. Solid-Phase Diffusion Mechanism for GaAs Nanowire Growth. *Nat. Mater.* **2004**, *3*, 677−681.

(13) Wang, K. C.; Yuan, G. D.; Wu, R. W.; Lu, H. X.; Liu, Z. Q.; Wei, T. B.; Wang, J. X.; Li, J. M.; Zhang, W. J. GaN Nanowire Arrays by a Patterned Metal-Assisted Chemical Etching. *J. Cryst. Growth* **2016**, *440*, 96−101.

(14) Morales, A. M.; Lieber, C. M. A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires. *Science* **1998**, *279*, 208−211.

(15) Manghi, F.; Calandra, C. Theoretical Investigation of the Fermi Level Pinning at the Sb-GaAs(110) Interface. *Vacuum* **1990**, *41*, 693−694.

(16) Sankey, O. F.; Allen, R. E.; Dow, J. D. Si-Transition-Metal Schottky Barriers - Fermi-Level Pinning by Si Dangling Bonds at Interfacial Vacancies. *Solid State Commun.* **1984**, *49*, 1−5.

(17) Portz, V.; Schnedler, M.; Lymperakis, L.; Neugebauer, J.; Eisele, H.; Carlin, J. F.; Butte, R.; Grandjean, N.; Dunin-Borkowski, R. E.; Ebert, P. Fermi-Level Pinning and Intrinsic Surface States of $Al_{1-x}inxnd(10−10)$ Surfaces. *Appl. Phys. Lett.* **2017**, *110*, 022104.

(18) Kim, C.; Moon, I.; Lee, D.; Choi, M. S.; Ahmed, F.; Nam, S.; Cho, Y.; Shin, H. J.; Park, S.; Yoo, W. J. Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides. *ACS Nano* **2017**, *11*, 1588−1596.

(19) van Leest, R. H.; Mulder, P.; Bauhuis, G. J.; Cheun, H.; Lee, H.; Yoon, W.; van der Heijden, R.; Bongers, E.; Vlieg, E.; Schermer, J. J. Metal Diffusion Barriers for GaAs Solar Cells. *Phys. Chem. Chem. Phys.* **2017**, *19*, 7607−7616.

(20) Speckbacher, M.; Treu, J.; Whittles, T. J.; Linhart, W. M.; Xu, X.; Saller, K.; Dhanak, V. R.; Abstreiter, G.; Finley, J. J.; Veal, T. D.; Koblmüller, G. Direct Measurements of Fermi Level Pinning at the Surface of Intrinsically n-Type InGaAs Nanowires. *Nano Lett.* **2016**, *16*, 5135−5142.

(21) Upadhyay, S.; Jespersen, T. S.; Madsen, M. H.; Krogstrup, P.; NygÅrd, J. Low Temperature Transport in p-Doped InAs Nanowires. *Appl. Phys. Lett.* **2013**, *103*, 162104.

(22) Sabui, G.; Zubialevich, V. Z.; White, M.; Pampili, P.; Parbrook, P. J.; Mclaren, M.; Arredondo-Arechavala, M.; Shen, Z. J. GaN Nanowire Schottky Barrier Diodes. *IEEE Trans. Electron Devices* **2017**, *64*, 2283−2290.

(23) Jiang, N.; Wong-Leung, J.; Joyce, H. J.; Gao, Q.; Tan, H. H.; Jagadish, C. Understanding the True Shape of Au-Catalyzed GaAs Nanowires. *Nano Lett.* **2014**, *14*, 5865−5872.

(24) Tambe, M. J.; Ren, S.; Gradecak, S. Effects of Gold Diffusion on n-Type Doping of GaAs Nanowires. *Nano Lett.* **2010**, *10*, 4584−4589.

(25) Renard, V. T.; Jublot, M.; Gergaud, P.; Cherns, P.; Rouchon, D.; Chabli, A.; Jousseaume, V. Catalyst Preparation for CMOS-Compatible Silicon Nanowire Synthesis. *Nat. Nanotechnol.* **2009**, *4*, 654−657.

(26) Kauppinen, C.; Haggren, T.; Kravchenko, A.; Jiang, H.; Huhtio, T.; Kauppinen, E.; Dhaka, V.; Suihkonen, S.; Kaivola, M.; Lipsanen, H.; Sopanen, M. A Technique for Large-Area Position-Controlled Growth of GaAs Nanowire Arrays. *Nanotechnology* **2016**, *27*, 135601.

(27) Wang, Y.; Yang, Z.; Wu, X.; Han, N.; Liu, H.; Wang, S.; Li, J.; Tse, W.; Yip, S.; Chen, Y.; Ho, J. C. Growth and Photovoltaic Properties of High-Quality GaAs Nanowires Prepared by the Two-Source CVD Method. *Nanoscale Res. Lett.* **2016**, *11*, 191.

(28) Ruppert, C.; Thunich, S.; Abstreiter, G.; Fontcuberta, i. M. A.; Holleitner, A. W.; Betz, M. Quantum Interference Control of Femtosecond, Ma Current Bursts in Single GaAs Nanowires. *Nano Lett.* **2010**, *10*, 1799−1804.

(29) Dunaevskiy, M.; Dementyev, P.; Egorov, V.; Polyakov, N.; Samsonenko, Y.; Cirlin, G.; Titkov, A. Measurements of Current-Voltage Characteristics of Separate Single GaAs Nanowhiskers. *Phys. Status Solidi C* **2009**, *6*, 2701−2703.

(30) Wang, Y.; Duan, C.; Peng, L. M.; Liao, J. H. Dimensionality-Dependent Charge Transport in Close-Packed Nanoparticle Arrays: From 2d to 3d. *Sci. Rep.* **2015**, *4*, 7565.

(31) Han, N.; Wang, F.; Hui, A. T.; Hou, J. J.; Shan, G.; Xiu, F.; Hung, T.; Ho, J. C. Facile Synthesis and Growth Mechanism of Ni-Catalyzed GaAs Nanowires on Non-Crystalline Substrates. *Nanotechnology* **2011**, *22*, 285607.

(32) Zhang, G.; Tateno, K.; Sanada, H.; Tawara, T. Synthesis of GaAs Nanowires with Very Small Diameters and Their Optical Properties with the Radial Quantum-Confinement Effect. *Appl. Phys. Lett.* **2009**, *95*, 123104.

(33) Martelli, F.; Rubini, S.; Piccin, M.; Bais, G.; Jabeen, F.; De Franceschi, S.; Grillo, V.; Carlino, E.; D'Acapito, F.; Boscherini, F.; et al. Manganese-Induced Growth of GaAs Nanowires. *Nano Lett.* **2006**, *6*, 2130−2134.

(34) Premchander, P.; Jayavel, R.; Arivuoli, D.; Baskar, K. Effect of SeS_2 Treatment on the Surface Modification of GaAs and Adhesive Wafer Bonding of Gaas with Silicon. *J. Cryst. Growth* **2004**, *263*, 454−458.

(35) Harmand, J. C.; Patriarche, G.; Pere-Laperne, N.; Merat-Combes, M. N.; Travers, L.; Glas, F. Analysis of Vapor-Liquid-Solid Mechanism in Au-Assisted GaAs Nanowire Growth. *Appl. Phys. Lett.* **2005**, *87*, 203101.

(36) Paiano, P.; Prete, P.; Lovergine, N.; Mancini, A. M. Size and Shape Control of GaAs Nanowires Grown by Metalorganic Vapor Phase Epitaxy Using Tertiarybutylarsine. *J. Appl. Phys.* **2006**, *100*, 094305.

(37) Wacaser, B. A.; Dick, K. A.; Johansson, J.; Borgstroem, M. T.; Deppert, K.; Samuelson, L. Preferential Interface Nucleation: An Expansion of the VLS Growth Mechanism for Nanowires. *Adv. Mater.* **2009**, *21*, 153−165.

(38) Han, N.; Wang, F.; Hou, J. J.; Xiu, F.; Yip, S. P.; Hui, A. T.; Hung, T. F.; Ho, J. C. Controllable p−n Switching Behaviors of GaAs Nanowires Via an Interface Effect. *ACS Nano* **2012**, *6*, 4428−4433.

(39) Han, N.; Yang, Z.; Shen, L.; Lin, H.; Wang, Y.; Pun, E. Y. B.; Chen, Y.; Ho, J. C. Design and Fabrication of 1-D Semiconductor

Nanomaterials for High-Performance Photovoltaics. *Science Bulletin* **2016**, *61*, 357−367.

(40) Guha, S.; Arora, B. M.; Salvi, V. P. High Temperature Annealing Behaviour of Schottky Barriers on GaAs with Gold and Gold-Gallium Contacts. *Solid-State Electron.* **1977**, *20*, 431−432.

(41) Chia, A. C. E.; Lapierre, R. R. Analytical Model of Surface Depletion in GaAs Nanowires. *J. Appl. Phys.* **2012**, *112*, 063705.

(42) Han, N.; Hou, J. J.; Wang, F.; Yip, S.; Yen, Y. T.; Yang, Z. X.; Dong, G.; Hung, T.; Chueh, Y. L.; Ho, J. C. GaAs Nanowires: From Manipulation of Defect Formation to Controllable Electronic Transport Properties. *ACS Nano* **2013**, *7*, 9138−9146.

(43) Lide, D. R. *CRC Handbook of Chemistry and Physics*, 90th ed.; CRC Press: Boca Raton, FL, 2010; pp 12−114.

(44) von Wenckstern, H.; Biehne, G.; Rahman, R. A.; Hochmuth, H.; Lorenz, M.; Grundmann, M. Mean barrier height of Pd Schottky contacts on ZnO thin films. *Appl. Phys. Lett.* **2006**, *88*, 092102.

(45) Hjort, M.; Lehmann, S.; Knutsson, J.; Zakharov, A. A.; Du, Y. J. A.; Sakong, S.; Timm, R.; Nylund, G.; Lundgren, E.; Kratzer, P.; Dick, K. A.; Mikkelsen, A. Electronic and Structural Differences between Wurtzite and Zinc Blende InAs Nanowire Surfaces: Experiment and Theory. *ACS Nano* **2014**, *8* (12), 12346−12355.