PAPER

Selective n-type doping in graphene *via* the aluminium nanoparticle decoration approach†

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Selective and reliable n-type doping as well as tuning the Dirac point of graphene are important for the realization of high-performance complementary circuits. In this work, we present a simple but effective technique to left shift the Dirac point of graphene transistors to induce n-type doping *via* thermal decoration of Al nanoparticles. The decorated discrete nanoparticles are uniformly distributed on the top of the graphene channel surface with consistent size and shape. Detailed electrical measurements reveal that the decoration can efficiently shift the Dirac point of graphene towards negative gate voltages along with the improved on/off current ratio and excellent air-stability. All these further indicate the technological potency of this doping technique for the fabrication of future CMOS graphene electronics.

Introduction

Due to its unique chemical, electrical, optical and thermo-mechanical properties, graphene has attracted a widespread interest in recent years.[1–10] However, numerous practical technological applications of graphene are inherently handicapped by its semi-metallic nature. For example, selective doping as well as tuning the Dirac point of graphene are key areas drawing tremendous attention because a reliable control in carrier concentration is necessary to construct integrated graphene devices with complicated architectures such as diodes, transistors and logic gates.[11–17] Even though both p- and n-type doping are equally important for the development of high-performance graphene-based electronic devices, the realization of n-type semiconducting graphene is imperative for complementary circuits since the p-type graphene channel can be readily prepared by chemical vapour deposition (CVD) growth because of the unintentional p-type doping induced by the oxygen and moisture or solution based transfer processes.[18–25] Therefore, various methods have been proposed to fabricate

n-type graphene transistors, employing the surface dopants of nitrogen or phosphorus atoms[26–31] or metallic thin films.[32–34] Doping with the incorporation of nitrogen and phosphorus dopants into the carbon lattice can lead to n-type transport characteristics in graphene;[22,35] however, at the same time, all these dopants can introduce defects into the lattice, which may deteriorate the resulting carrier mobility.[23,24] While in the thin film cases, Kim *et al.* have recently reported the n-type doping in graphene, utilizing the deposition of photo-patterned gold nanoparticles.[36] In any case, these fabricated n-type graphene devices have very limited air stability as they are sensitive to the influence of ambient environment. Therefore, achieving air-stable n-type semiconducting properties of graphene still remains a challenge. In this report, we present a simple but effective technique to left shift the Dirac point of graphene transistors inducing n-type doping *via* the thermal decoration of Al nanoparticles and Al_2O_3 passivation layer. The morphologies of these Al nanoparticles are carefully characterized with atomic force microscopy (AFM). Combined with the detailed electrical measurements, it is revealed that the Al-decorated graphene devices exhibit an impressive on/off current ratio, and the corresponding electrical properties are highly dependent on the dimension of deposited Al nanoparticles.

Experimental section

Growth and transfer of monolayer graphene

Here, we successfully grew monolayer graphene using low pressure CVD on copper foils and optimized the graphene transfer onto the Si/SiO_2 substrates. In brief, copper foils were first annealed at 1000 °C for 30 to 45 min in an H_2/Ar environment at a process pressure of 300 mTorr. Then, methane was introduced through the feeding of $CH_4/Ar/H_2$ mixture at a

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higher process pressure of 500 mTorr for 30 min. Next, the entire system was cooled down to room temperature, where graphene percolated on the surface of copper foils. The foils were covered by poly(methyl methacrylate) (PMMA) to protect the top surface, while O_2 plasma treatment was performed on the backside to remove any graphene growth. Later, the copper foils were etched in the commercial copper etchant for 30 min, the graphene layer was then transferred to 10% HCl/DiH_2O solution and later rinsed with DiH_2O for multiple times. Finally, the graphene layer was transferred onto the Si/SiO_2 substrates with 50 nm thick thermal grown oxide as the gate-dielectric and annealed at 500 °C for 2 h in an ambient environment of H_2/Ar (150 SCCM and 400 SCCM, respectively) to remove PMMA.

Fabrication of graphene field-effect transistors

The back-gated graphene field-effect transistors (FETs) studied in this work were fabricated as follows. The source–drain electrode region was first patterned by photolithography. Cr (5 nm) and Au (90 nm) metal layers were deposited onto the photoresist pattern by electron beam evaporation, which was followed by a lift-off process. After the metal patterning, the graphene channels [device type A: channel width (W) = 3 μm, channel length (L) = 10 μm and device type B: W = 5 μm, L = 10 μm] were defined utilizing photolithography and subsequent reactive ion etching (RIE) in an oxygen ambient environment. The RIE was performed for 30 s at 100 W and room temperature with 5 mTorr of O_2. Afterwards, Al nanoparticles were decorated onto the graphene channels with different nominal thicknesses employing thermal evaporation. Notably, the 30 nm thick Al_2O_3 protective layer was also deposited to prevent Al nanoparticles from further oxidation.[37] The schematic of the Al decorated graphene FET device structure is illustrated in ESI Fig. S1(a),† while the corresponding top-down SEM image is depicted in Fig. S1(b).†

Results and discussion

As shown in the microscopy image in Fig. 1a, we have successfully synthesized and transferred the large-scale monolayer graphene onto the Si/SiO_2 substrates. The AFM image (Fig. 1b) indicates the corresponding grain structure and wrinkles of the transferred graphene. From the AFM analysis, the thickness of this monolayer graphene is about 1 nm. Notably, the Raman mapping of this graphene in Fig. 1c gives the very weak intensity of D band at ~1350 cm^{-1}, which suggests the minimal defect concentration here. In addition, the 2D band is very sharp and symmetric at ~2660 cm^{-1} with the full-width-at-half-maximum (FWHM) of ~39 cm^{-1} as well as the intensity ratio of G/2D, which is less than 1. All these confirm the excellent crystal quality of the as-synthesized graphene layer utilized in this work.[38]

In order to investigate the effect of Al nanoparticle decoration on the fabricated graphene FETs, various thicknesses of Al film were deposited on the graphene layer. As presented in AFM images in Fig. 2, the topography of three different decoration thicknesses are revealed, which corresponds to the nominal Al
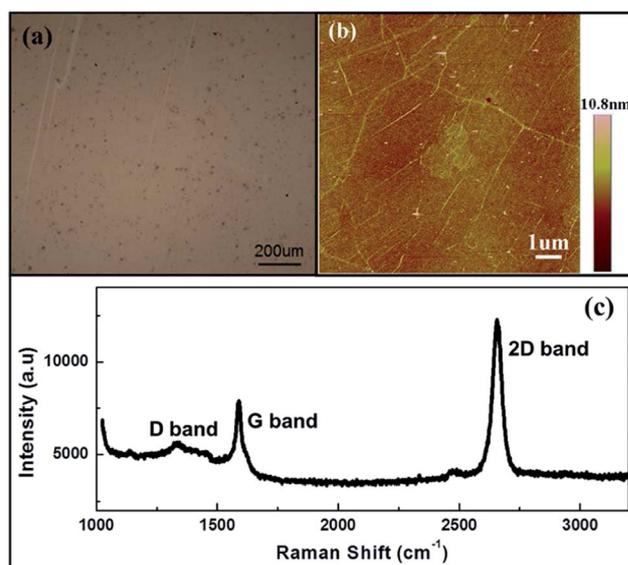

Fig. 1 Characterization of the synthesized and transferred graphene layer. (a) Optical microscope image, (b) AFM topography image and (c) Raman spectrum (514 nm wavelength excitation).
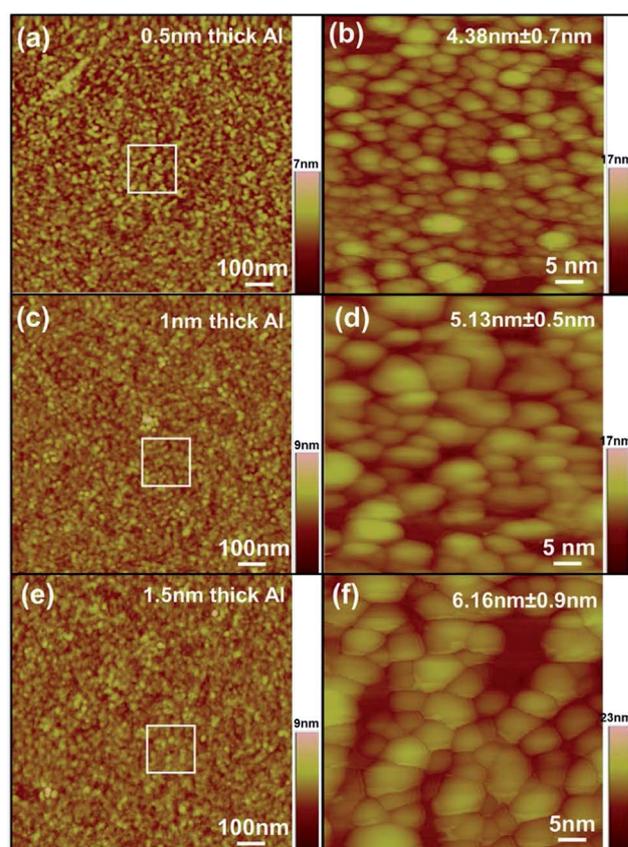

Fig. 2 AFM topography images of graphene layer with different Al decoration thicknesses. (a) and (b) 0.5 nm, (c) and (d) 1.0 nm, (e) and (f) 1.5 nm. White colored square boxes designate the zoom-in characterization region. Statistics of the decorated nanoparticle size are given in the top right corner.

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deposition thickness of 0.5, 1.0 and 1.5 nm, respectively. Based on more than 50 individual particles from AFM images, the average size of Al nanoparticles is determined to be 4.38 nm ± 0.7 nm, 5.13 nm ± 0.5 nm and 6.16 nm ± 0.9 nm (ESI Fig. S2†). This relatively narrow particle size distribution is remarkably good considering the simplicity of this simple thermal evaporation technique as compared to the variation of commercially available colloidal metal nanoclusters. Importantly, this reasonably good particle size control can give us the capability to modulate the decorated cluster dimension in subsequent studies.

At the same time, two kinds of FET devices (device type A with a channel width of 3 μm and device type B with a channel width of 5 μm) were prepared for electrical transport measurements before and after nanoparticle decoration in order to evaluate the decoration effect on different device geometries. During the FET measurement, 1.0 V bias was applied between the source and drain while a variable gate bias (V_{GS}) ranging from −20 to +40 V, was applied to the highly doped Si, which served as a back-gate. Sequentially, the source–drain current (I_{DS}) was monitored as a function of V_{GS} to assess the corresponding transfer characteristics of graphene FETs. As depicted in Fig. 3, the graphene devices exhibit p-type behaviour due to the unintentional doping from defects and pre-existing adsorbates, such as the oxygen and water in air.[18–25] In this case, the black curves give the I_{DS}–V_{GS} relationship of pristine graphene before the decoration. One can see that the I_{DS} increases slowly with decreasing V_{GS} and the on/off ratio is about 1.3. The gate dependence of maximum resistance defines the position of the Dirac point, which does not show up within the measured range. However, after the 1 nm Al decoration, the pure p-type characteristic is transformed into the ambipolar behaviour with significant n-type conduction, indicating a successful n-type doping in these devices (Fig. 3a and c). Also, the Dirac point is then shifted to ∼20 V and ∼10 V for device type A and B,

corresponding to the hole concentration of 1.78×10^{12} cm^{-2} and 0.87×10^{12} cm^{-2}, respectively (ESI†), and the on/off current ratio is enhanced to ∼4 to 6 times without any significant change in the on-current as compared to those before the decoration. It is noted that the n-type doping phenomenon is more pronounced for the wider device channel (ESI Fig. S3 and S4†), which is expected due to the suppressed edge effect as compared to the narrower ones because the oxygen plasma defined edges could behave as p-type dopants. In the future, edge passivation may be further required to improve the n-doping effect, especially for narrow channel graphene FETs. More importantly, the decorated devices show consistent electrical results even after ten days of exposure in the ambient, indicating the long-term air-stability with this simple doping technique.

To verify that the doping effect is coming from the Al decoration, not the protective Al_2O_3 layer, other devices with the same dimension were also deposited with only a pure 30 nm thick Al_2O_3 layer as the control. As illustrated in Fig. 3b and d, the Al_2O_3 layer cannot move the Dirac point; however, it improves the on/off current ratio to ∼4 to 6 times due to the passivating effect in minimizing the exposure to ambient environment, which helps to eliminate the hydroxyl, oxygen and water related molecules adsorbed onto the graphene channel.[37,39] Another set of control samples were also performed on the same device structure without the active graphene channel layer, and as expected no current can be measured (ESI Fig. S5†), which indicates that our nanoparticles are still disconnected at the decoration thickness of 1 nm. All these experiments confirm the role of Al nanoclusters in the n-type doping and left-shifting of the Dirac point of graphene.

It should also be noted that the doping effect of Al nanoparticle decoration on graphene FETs is observed to highly depend on the particle size. As shown in Fig. 4, when the nominal decoration thickness is increased from 0.5 to 1.5 nm, the Dirac point is first shifted towards the negative voltages from +20 to +10 V and then moved back to +30 V. The maximum left-shifting of the Dirac point is corresponded to the decoration thickness of 1 nm, which suggests that because the nanoparticle size is too small (i.e. 0.5 nm thickness), the isolated nanoparticles have insignificant contact area with the graphene channel to achieve the maximum doping effect; whereas for the very large particle size (i.e. 1.0 nm thickness), the nanoparticles start to coalescence towards a continuous film for reducing the electronic doping level of graphene such that the Dirac point is moved back to the positive gate voltages. We notice that in a previous numerical study,[40] the Fermi level shift of graphene illustrated a strong dependence on the graphene–metal surface separations because the different distance imply different intensities of interactions between the two bodies. In this case, when the Al gets thicker and become a quasi-film, the equilibrium separations between graphene and Al gets larger because of the surface wrinkling/fluctuation of the graphene. Therefore, the doping effect of Al gets weaker in this manner. Further increase of the Al particle size would form a continuous conducting mesh turning the graphene into a metal.
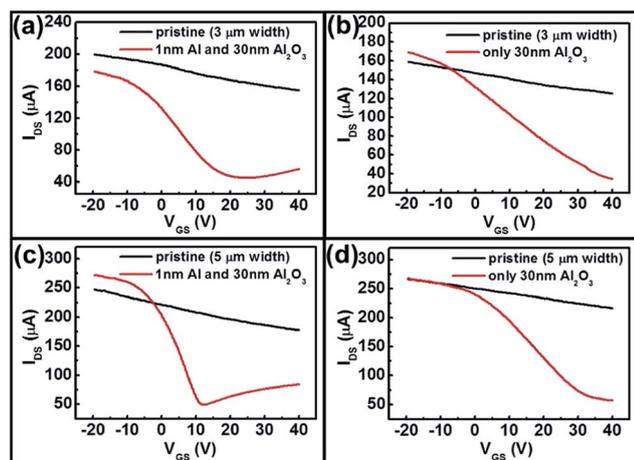

Fig. 3 Transfer characteristics of Al nanoparticle decorated graphene FETs. (a) and (c) decoration thickness of 1.0 nm capped with 30 nm Al_2O_3 for the device type A (3 μm channel width) and device type B (5 μm channel width), respectively, (b) and (d) no decoration capped with only 30 nm Al_2O_3 for device type A and B, respectively.

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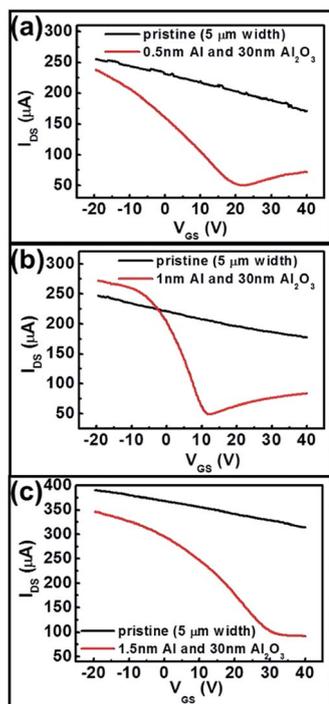J. Mater. Chem. C, 2014, 2, 5417–5421 | 5419

Fig. 4 Transfer characteristics of Al nanoparticle decorated graphene FETs with different decoration thicknesses. (a) 0.5 nm, (b) 1.0 nm and (c) 1.5 nm.

To intuitively understand the physical mechanism of this Al nanoparticle decoration, Fig. 5 shows the effective potential along the graphene/nanoparticle contact interface. It is well-known that the work function of Al nanoparticles ($W_{Al} = 4.28$ eV) is lower than that of pristine graphene ($W_G = 4.6$ eV). When the nanoparticles are deposited onto the graphene surface, the large negative work function difference ($W_{Al} - W_G$) would result in an upshift of the graphene Fermi energy. Specifically, the left valley represents the potential of graphene, while the right valley represents the potential of Al. Driving from the potential difference, electrons would be donated from the Al particles and will be injected into the g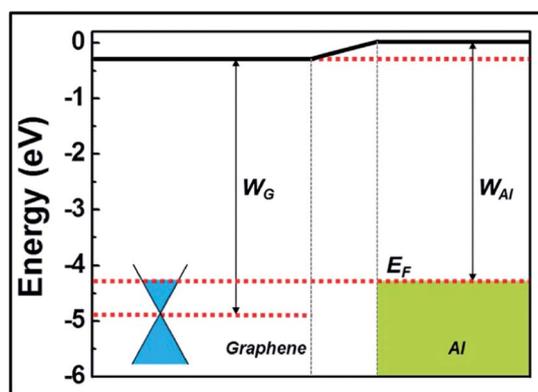raphene, creating a built-in electric field in the same direction. Thus, the transferred electrons will raise the Fermi level and achieve n-type doping in the graphene here.

Apart from Al, the doping effect of other metal nanoparticle decorations, such as Sn, has also been investigated. It is found that the Sn decoration could also shift the Dirac point of the same graphene FETs to +20 V, which was not as efficient as compared to the n-type doping observed by Al (ESI Fig. S6†). It is because of the fact that Sn has a work function of 4.42, which is larger than that of Al, and that the induced Fermi energy up-shift of graphene would not be as large to result in the same amount of energy transfer for the n-type doping. More studies on further controlling this doping technique on graphene are currently in ongoing.

Conclusions

In conclusion, a simple n-type doping technique to left shift the Dirac point of graphene transistors *via* the thermal decoration of Al nanoparticles is presented. The morphologies of these Al nanoparticles on graphene are carefully characterized, suggesting that the particles are distributed with relatively uniform size and shape. Combined with the detailed electrical measurements, the decorated graphene devices exhibit an obvious left-shifting of the Dirac point, inducing the efficient n-type doping along with the impressive on/off current ratio and excellent air-stability. All these indicate the technological potency of this decoration technique for the reliable n-type doping for the future fabrication of graphene devices.

Acknowledgements

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Fig. 5 Schematic illustration of the relationship between Fermi energy and work function along the graphene/nanoparticle contact interface.

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