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Research Article

Gate Bias Stress Instability and Hysteresis Characteristics of InAs Nanowire Field-Effect Transistors

Changyong Lan,[⊥] SenPo Yip,[⊥] Xiaolin Kang, You Meng, Xiuming Bu, and Johnny C. Ho*

Cite This: *ACS Appl. Mater. Interfaces* 2020, 12, 56330–56337

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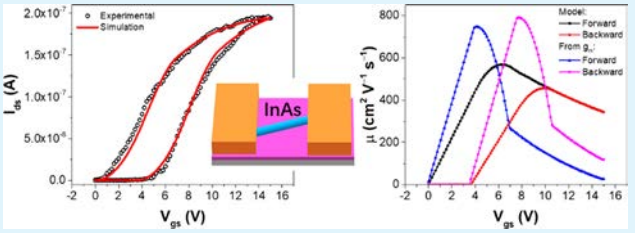
ABSTRACT: Because of the excellent electrical properties, III–V semiconductor nanowires are promising building blocks for next-generation electronics; however, their rich surface states inevitably contribute large amounts of charge traps, leading to gate bias stress instability and hysteresis characteristics in nanowire field-effect transistors (FETs). Here, we investigated thoroughly the gate bias stress and hysteresis effects in InAs nanowire FETs. It is observed that the output current decreases together with the threshold voltage shifting to the positive direction when a positive gate bias stress is applied, and vice versa for the negative gate bias stress. For double-sweep transfer characteristics, the significant hysteresis behavior is observed, depending heavily on the sweeping rate and range. On the basis of complementary investigations of these devices, charge traps are confirmed to be the dominant factor for these instability effects. Importantly, the hysteresis can be simulated well by utilizing a combination of the rate equation for electron density and the empirical model for electron mobility. This provides an accurate evaluation of carrier mobility, which is in distinct contrast to the overestimation of mobility when using the transconductance for calculation. All these findings are important for understanding the charge trap dynamics to further enhance the device performance of nanowire FETs.



KEYWORDS: *InAs, nanowire, field-effect transistor, bias stress, hysteresis*

INTRODUCTION

In the past few decades, due to the excellent properties arising from unique one-dimensional (1D) structures, single-crystalline semiconducting nanowires have been demonstrated with many promising applications for next-generation electronics and optoelectronics.[1−4] Particularly, the small band gap III–V nanowire (NW) materials, such as InAs, can be grown nonepitaxially and transferred onto any substrate for device utilization.[5−7] Once configured into transistors, InAs NWs exhibit the superior field-effect electron mobility of $>1 \times 10^4$ $cm^2\ V^{-1}\ s^{-1}$,[8,9] which is significantly higher than the one of Si, the major workhorse of the electronic industry. This makes InAs NWs promising channel materials for high-mobility field-effect transistors (TFTs) and high-frequency electronics.[10−12] Inevitably, because of the 1D characteristics of InAs NWs, they have an intrinsically large surface area-to-volume ratio, consisting of large amounts of surface states to significantly influence their electrical and optoelectronic properties and subsequently fabricated device performances.[13−16] For instance, the surface roughness of InAs NWs was observed to lead to substantial surface traps for carrier scattering and reduced carrier mobility.[8] At the same time, InAs NWs synthesized by chemical vapor deposition (CVD) always came with unstable native oxide layers,[8,17,18] which acted as surface charge traps, deteriorating their electrical properties.[18,19] These charge traps in the NWs would also lead to many instability phenomena of the NW-based FETs, such as gate bias stress effect[20,21] and hysteresis characteristics.[18,22−25] These instability effects not only make the accurate determination of many device performance parameters (e.g., carrier mobility, threshold voltage, etc.) challenging but also impose detrimental limitations on the practical applications of NW transistors. In this regard, it is important to investigate the origin of these instability issues in order to further the development of NW devices.

In this work, the gate bias stress instability and hysteresis characteristics of the InAs NW FETs are carefully examined. It is observed that the InAs NW devices demonstrate significant instability effects when applying both negative and positive gate bias stresses. To be specific, the device output current would decrease with the threshold voltage (V_T) shifting toward the positive direction when a positive gate bias stress is applied, whereas the current increases with the V_T moving toward the negative direction when a negative gate bias stress is applied. These gate bias stress instability effects even get more

Received: September 26, 2020
Accepted: November 24, 2020
Published: December 8, 2020

https://dx.doi.org/10.1021/acsami.0c17317
ACS Appl. Mater. Interfaces 2020, 12, 56330–56337

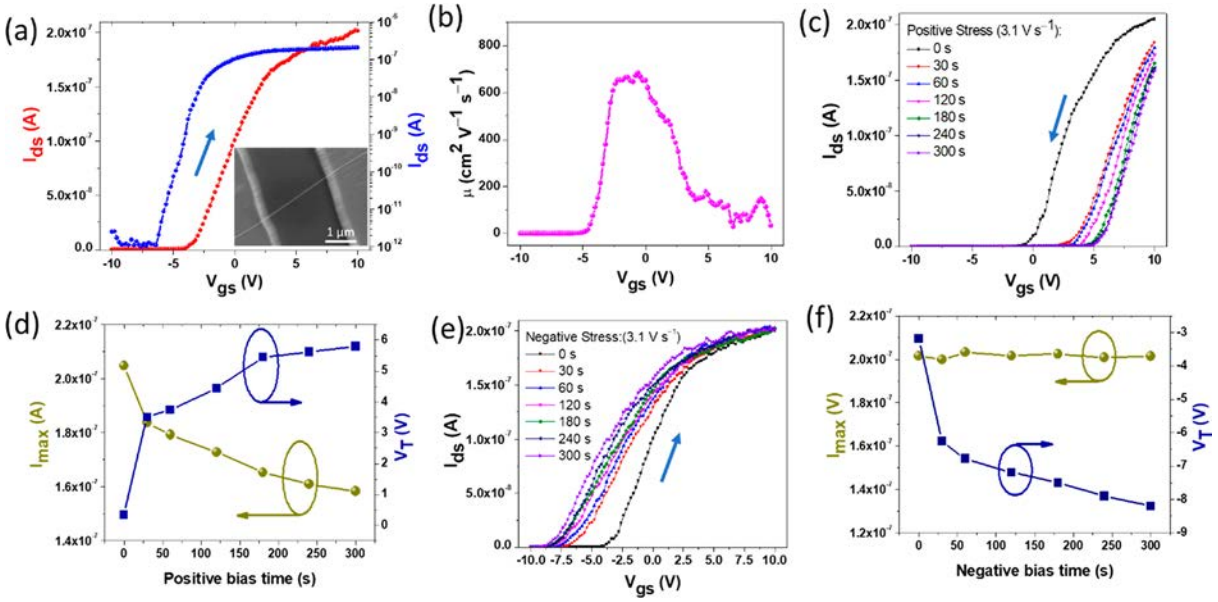


Figure 1. Electrical properties and gate bias stress effects of the InAs nanowire FET. (a) Transfer curves in linear and logarithmic plots. Inset shows the SEM image of the investigated device. (b) Electron mobility as a function of gate voltage. (c) Positive stress under different stress times. (d) Maximum source-drain current and threshold voltage as a function of positive bias stress time. (e) Negative stress under different stress times. (f) Maximum source-drain current and threshold voltage as a function of negative bias stress time. The bias voltages for positive and negative stresses are 10 and −10 V, respectively. The voltage sweeping rate is 3.1 V s^{-1}. The source-drain voltage is 20 mV for the measurements.

enhanced with the extension of the bias stress time. For the double-sweep current−voltage (I−V) measurements, substantial hysteresis is seen, in which it is highly dependent on the sweeping rate. The slower the sweeping rate gives the larger hysteresis loop. On the basis of the complementary electrical characterizations, charge traps are found to be the dominant factor for these instability and hysteresis issues of NW FETs. By developing a rate equation for electron density together with an empirical model for electron mobility, the hysteresis characteristics of NW devices can be theoretically reproduced and understood. In addition, it is also realized that the peak electron mobility of NW devices is usually overestimated when using the transconductance for mobility calculation. All these findings provide valuable guidelines for the accurate evaluation of the NW transistor performance as well as insights for the enhanced design of NW devices for practical utilization.

EXPERIMENTAL SECTION

The InAs NWs were synthesized by solid-source chemical vapor deposition as reported in previous works.[17] After the NW synthesis, the NWs were first dispersed in an anhydrous ethanol solution and then drop-casted onto the Si/SiO_2 (50 nm thermal oxide) substrate for the subsequent device fabrication process. Specifically, standard photolithography was carried out to define the region for source and drain electrodes. Before Ni electrodes deposition, the NWs were treated with 1% HF solution in order to eliminate the oxidation layer. Electron-beam evaporation was used to deposit Ni electrodes, followed by the lift-off process. After that, the electrical characteristics of the fabricated NW FETs were measured in a vacuum probe station with a base pressure down to 1×10^{-4} Pa and in dark condition. A semiconductor analyzer (Keysight B1500A) was used for the electrical measurements. A scanning electron microscope (SEM, Quanta 450 FEG, FEI) was also employed to study the surface morphology of the obtained NW devices.

RESULTS AND DISCUSSION

Here, the electrical properties of the typical InAs NW FET were first carefully evaluated with the corresponding SEM image of the device depicted in Figure 1a inset. The FET showed typical n-type semiconducting behavior, in which the source-drain current (I_{ds}) increased once the applied gate bias (V_{gs}) exceeded the threshold voltage (V_T) of the device (Figure 1a). In this case, the device operated in depletion mode because the V_T had a negative value and the FET functioned at its ON state when $V_{gs} = 0$. The mobility of the device could then be estimated by the following equation:

$$\mu = g_m \frac{L^2}{C_{ox}} \frac{1}{V_{ds}} \quad (1)$$

where g_m is the transconductance that is defined as $\partial I_{ds}/\partial V_{gs}$, L is the channel length, C_{ox} is the gate capacitance, and V_{ds} is the source-drain voltage. In particular, for an NW channel length of 2.5 μm, NW diameter of 30 nm, V_{ds} of 20 mV, and gate capacitance (C_{ox}) determined from the finite element simulation,[24] the field-effect electron mobility of the NW device as a function of gate voltage is shown in Figure 1b. It is clear that the electron mobility gradually increased when the FET was at its ON state. Then, the mobility reached its peak value (688 cm^2 V^{-1} s^{-1}) and started to decrease with the gate voltage. The increasing mobility at the initial stage is known to be due to the enhanced Coulomb screening with the increased carrier density, whereas the decreasing mobility at high gate voltage comes from the surface scattering.[8,26] The statistical data of the peak mobility of the InAs NW device from tens of different NW devices are shown in Supporting Information Figure S1. All these electrical characteristics are typical to the state-of-the-art InAs NW FETs reported in the literature, which are essential for the successive studies.

After that, the effect of gate bias stress on the NW FET performance was systematically evaluated. For the positive gate

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ACS Appl. Mater. Interfaces 2020, 12, 56330−56337

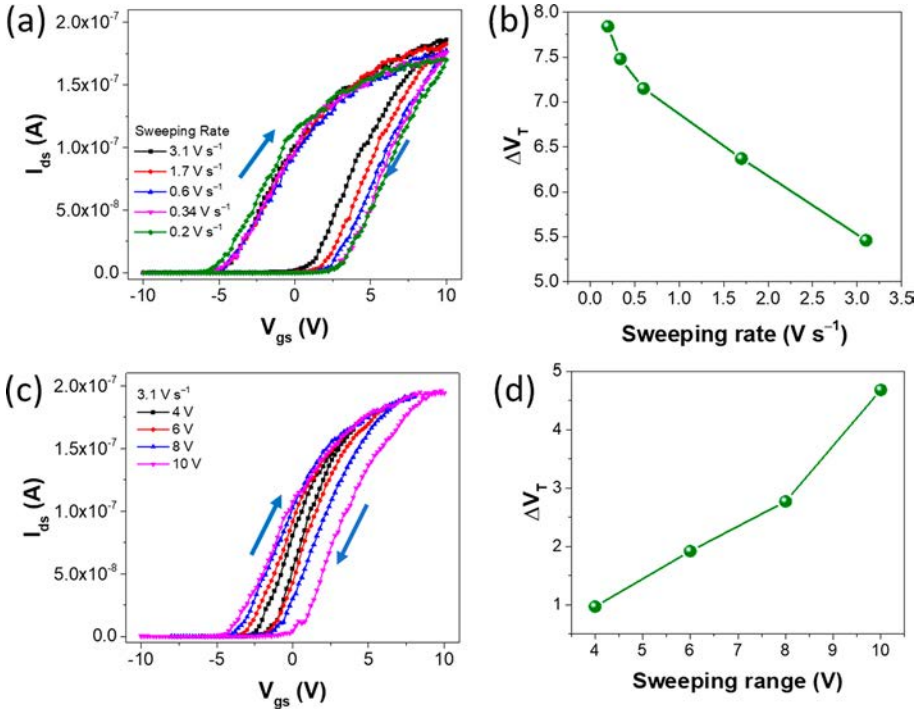

Figure 2. Hysteresis behaviors of the InAs nanowire FET. (a) Double-sweep transfer curves with different sweeping rates. (b) Threshold voltage difference as a function of sweeping rate. (c) Double-sweep transfer curves with different sweeping ranges. (d) Threshold voltage difference as a function of sweeping range. The V_{ds} is 20 mV for the measurements.

bias stress, a constant gate voltage (10 V) was applied on the device with a stress time that varied from 0 to 300 s and a fixed sweeping rate (3.1 V s^{-1}). For the negative gate bias stress, a constant negative gate voltage (−10 V) was applied. For each measurement, 1 h wait time was used to ensure the device recovered from the previous gate bias stress measurement. As shown in Figure 1c, the transfer curves keep shifting to the positive direction as the positive gate bias stress time increases. Under the prolonged positive gate bias stress, the curves almost coincide. For a clearer understanding of the variation of transfer curves under different positive bias stress times, the corresponding maximum source-drain current as well as the threshold voltage are extracted and depicted in Figure 1d, accordingly. The maximum current exhibits a fast decrease at the short bias stress time, while the decreasing speed slows down with the longer bias stress time. Similarly, the trend of the threshold voltage is that it first increases rapidly and then the increase slows down for the extended positive gate bias stress. On the other hand, when the negative gate bias stress is applied to the NW device, the transfer curves progressively move to the negative direction, as shown in Figure 1e. Interesting, there are almost no changes for the maximum current, but the threshold voltage shifts to the negative direction for the increasing negative gate bias stress time, as indicated in Figure 1f. In general, the gate bias stress effect is mostly attributed to the charge traps that exist on the NW channel surface.[16,20,21,27] As all the electrical measurements were carried out under vacuum, the adsorbed molecules should not be the main reason for contributing the charge traps. In this manner, the native oxide on the InAs NW surface is believed to be the origin of these traps.[28] Moreover, the SiO_2 gate dielectric may also provide charge traps and contribute trap states for the NW device.[29] Considering there are some traps that are filled with electrons (n_{t0}) in the initial state with a total trap concentration of N_t, the gate-induced electron density (N) can be expressed as the following:

$$N = n + n_{t0} = \kappa \cdot (V_{gs} - V_{T0}) \tag{2}$$

where n is the free electron density, V_{gs} is the gate voltage, $\kappa = \frac{C_{ox}}{\pi r^2 L}$, and r is the radius of the NW. V_{T0} represents the value of the threshold voltage in the initial state. Under the positive gate bias stress, the charge traps are gradually filled with electrons such that the concentration of trapped electrons (n_t) increases with the positive gate bias stress time. In other words, the free electron density decreases with the positive gate bias stress time, leading to the decrease of the current. In addition, the trapped electrons can act to electrostatically reduce the electron density in the channel, further reducing the current.[15,16] When the gate bias stress time is long enough, n_t would approach N_t. In this way, n will become $N - N_t$, where the free electron density does not change with the gate bias stress time anymore. As a result, it is important to evaluate the decay time of the current in order to determine the positive gate bias stress time when all the traps are filled. This decay time can be obtained from the measured time-dependent current curve (Figure S4), in which it is determined to be ~318 s for the InAs NW device investigated here. This result is perfectly consistent with the time achieved for the saturation of the maximum current under the prolonged gate bias stress, as shown in Figure 1d. This relatively long decay time indicates that there is a slow trapping process that exists within the NW device. Because of the presence of the trapped electrons, the measured threshold voltage can be evaluated as follows:

$$V_T = V_{T0} + \frac{n_t}{\kappa} \tag{3}$$

https://dx.doi.org/10.1021/acsami.0c17317
ACS Appl. Mater. Interfaces 2020, 12, 56330−56337

Hence, V_T shows a similar trend with n_t, being consistent with the results discussed earlier. Under the negative gate bias stress, n_t would decrease with the gate bias stress time, leading to the decreasing threshold voltage as expected. During the sweeping from negative to positive gate bias, the traps would be gradually filled when the gate voltage exceeds the threshold voltage (i.e., equivalent to the positive gate bias stress). On the basis of the device transfer characteristics, the amounts of filled traps are almost the same for different negative gate bias stress times at the maximum gate voltage (V_{gs_m}) of 10 V. In fact, the trapping rate of electrons can be expressed by the analytical equation below:[30]

$$R_t = Svn(N_t - n_t) \tag{4}$$

where S is the capture cross section and v is the thermal velocity such that $\frac{1}{2}mv^2 = k_BT$. The capture rate is fast at the initial state, which eventually decreases when the traps are partly filled. The longer negative gate bias stress time would lead to a larger value of $(N_t - n_t)$; hence, it results in the larger capture rate. Consequently, although the applied gate bias stress time is different, the amount of final captured electrons may be the same, leading to almost the same current at the V_{gs_m}. Similar gate bias stress effects are also observed in other InAs NW-based FETs (see Figure S2), indicating the same mechanism controlling the gate bias stress effect.

Apart from the gate bias stress effects, the hysteresis characteristics of the NW FETs were also thoroughly studied. For the measurements of double-sweep transfer curves, the gate voltage is first swept from negative to positive bias (i.e., forward sweeping) and then swept back from positive to negative bias (i.e., backward sweeping). The double-sweep transfer curves of the typical NW FET under different sweeping rates are shown in Figure 2a. It is obvious that the hysteresis is enlarged at the slow sweeping rates. To quantify the hysteresis effect, the threshold voltage difference (ΔV_T) between forward and backward sweepings is employed to examine the magnitude of hysteresis. In this way, the extracted ΔV_T as a function of sweeping rate is compiled in Figure 2b, where ΔV_T is observed to decrease with the increasing sweeping rate. When the gate voltage is smaller than the threshold voltage V_T, the sweeping is equivalent to the negative gate bias, whereas for a gate voltage larger than V_T, the sweeping is equivalent to the positive gate bias. The appearance of the hysteresis can then be accounted for as follows: in the initial forward sweeping, the FET is negatively gate-biased, and the threshold voltage would shift to the negative bias direction. In the backward sweeping, the FET is positively gate-biased, leading the transfer curve to shift to the positive bias direction. As a result, the hysteresis effect appears in the transfer curves. Furthermore, the difference of the hysteresis becomes smaller for the slow sweeping rates. With a slow sweeping rate, the charge traps can be nearly fully filled, leading to almost the same hysteresis loop for all the slow sweeping rates. Notably, for the backward sweeping, the transfer curve shifts are observed to shift to the positive bias direction with the decreasing sweeping rate, and they eventually coincide for all the slow sweeping rates. This result indicates that the free carrier density (n) would be larger for the fast sweeping rate than that for the slow sweeping rate when V_{gs} is between V_T and V_{gs_m}, considering that the carrier density is the dominant factor to control the current. In this way, more electrons are trapped at the same V_{gs} for the slow sweeping rate under the backward sweeping, which can be explained by the equivalent longer gate bias stress time for the slow sweeping rate.

Besides, the hysteresis phenomena of the NW device can also be affected by the sweeping range of the applied gate bias, as shown in Figure 2c. It is clear that the hysteresis would get enlarged when a wider sweeping range is utilized. In this case, the ΔV_T increases with the increasing sweeping range, as presented in Figure 2d. In view of the equivalent gate bias stress effect induced by the gate sweeping, the observed phenomenon can be attributed to the larger sweeping range, in which the longer gate bias stress time and hence the larger hysteresis resulted. Similar behavior can also be observed in other InAs NW-based FETs (see Figure S3), indicating the universal hysteresis effect of these devices.

To shed light on the underlying mechanism behind the hysteresis phenomena, it is necessary to provide a theoretical model in order to explain the observed behaviors. Because charge trapping is well-recognized as the key factor for the hysteresis, a rate equation was then employed to describe the trapping process during the sweeping. To be specific, when the traps are not fully filled, the change of the free carrier density can be expressed as follows:

$$\frac{\partial n}{\partial t} = \alpha\gamma v_s - \frac{n}{\tau} \tag{5}$$

where $\gamma = 4C_{ox}/(\pi d^2 Lq)$, d is the diameter of the nanowire, L is the channel length, q is the charge of an electron, v_s is the sweeping rate, τ is the lifetime of electrons that can be trapped ($\tau = 1/R_t$), and α is an average attenuation coefficient for the forward sweeping and an enhancement coefficient for the backward sweeping. It should be noted that the sign of v_s is positive for forward sweeping while it is negative for backward sweeping. The first term on the right-hand side of eq 5 is caused by the gate voltage sweeping, while the second term is attributed to the electron trapping effect. Equation 5 is only valid when the traps are not fully occupied by electrons. For both forward and backward sweepings, the trapped electrons can actually act as extra gate charges, reducing and enhancing the gate control ability for forward and backward sweepings, respectively. The equivalent gating effect of the trapped charges has been widely observed in low-dimensional photodetectors as a photogating effect.[15,16,27,31,32] Thus, an extra coefficient α is introduced to account for the effect of gate charges. In this case, the average carrier lifetime can be obtained from the time-dependent current, which is determined to be ~318 s (Figure S4).

Because the device current is proportional to both carrier mobility and density, the carrier mobility should be known in order to evaluate the value of the current. For nanowires, the carrier mobility always has a complex relationship with the gate voltage.[26,33,34] In general, when the gate voltage increases, the carrier mobility rises and reaches a peak value, then decreases rapidly, as seen in Figure 1b. To make the discussion simple, an empirical formula is used to model the carrier mobility (see the detailed discussion in the Supporting Information and Figure S5). This way, the current can be described as follows:

$$I_{ds} = qA\frac{V_{ds}}{L}n\mu \tag{6}$$

where A is the cross-sectional area of the nanowire. As a result, the device current can be simulated as a function of the gate

https://dx.doi.org/10.1021/acsami.0c17317
ACS Appl. Mater. Interfaces 2020, 12, 56330−56337

voltage. Detailed information can be found in the Supporting Information.

Because the coefficient α has an important role for determining the simulation results, it is necessary to first discuss and understand the effect of α here. When the trapped electron-induced gating effect is not taken into consideration, the hysteresis of the transfer curves can still be reproduced (Figure 3a), where the hysteresis is only due to the electron

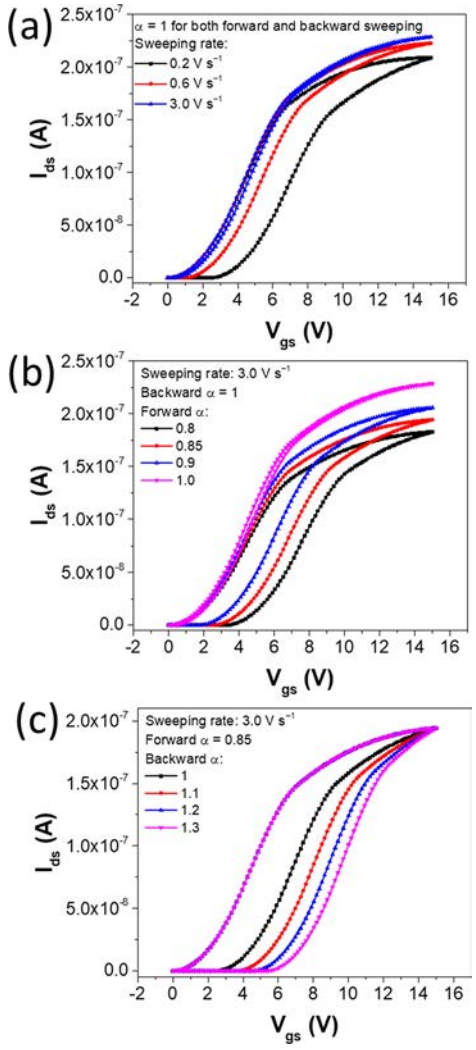

Figure 3. Effect of the coefficient α on the simulated transfer curves of the InAs nanowire FET. (a) α = 1 with different sweeping rates. (b) α changes from 0.8 to 1.0 for the forward sweeping and then remains 1 for the backward sweeping. (c) α changes from 1.0 to 1.3 for the backward sweeping and then remains 0.85 for the forward sweeping. In the simulation, the diameter of the InAs nanowire is 30 nm, the SiO_2 dielectric is 50 nm, and the V_{ds} is 20 mV.

trapping. However, this simulated result is not consistent with the experimental finding obtained, as shown in Figure 2a. In the simulation, there is only a small hysteresis observed for the fast sweeping rate, which is contradictory to the experimental finding that a significant hysteresis is attained. Therefore, the trapped electron-induced gating effect must be taken into serious consideration. In the forward sweeping, the trapped electrons can induce an equivalent negative gate voltage, reducing the gating effect. Thus, the value of α should be set to <1. If only the equivalent gating effect is considered for the forward sweeping, an enlarged hysteresis can be observed, as shown in Figure 3b. In fact, the output current decreases with the decreasing value of α, which is consistent with the reducing gating effect of the trapped charges. On the contrary, for the backward sweeping, the trapped electrons can enhance the depletion of the electrons in the channel. In this way, the value of α should be >1. As given in Figure 3c, the increasing value of α accelerates the decay of the current, being in perfect agreement with the enhanced depletion effect of the trapped electrons. This understanding of the coefficient α would provide important knowledge of the trapped electron-induced gating effect for subsequent studies.

By knowing the effect of α on a quantitative basis, the transfer characteristics of NW FETs can then be simulated well by tuning the value of α. Because the exact value of α is unknown, the value of α is thoroughly searched in order to satisfy the experimental results. As depicted in Figure 4a, the effect of the sweeping rate on the hysteresis is simulated, which is consistent with the experimental results (Figure 2a). To be specific, the smaller α and the larger α values are required to be utilized for forward and backward sweepings, respectively, for the slow sweeping rate. These values agree perfectly with the equivalent gating effect of the trapped electrons discussed earlier. At the same time, the simulated transfer curves with different sweeping ranges are shown in Figure 4b. It is noted that these curves exhibit a significant variation with different sweeping ranges for the backward sweeping, being consistent with the experimental results as shown in Figure 2c, whereas the observation is totally different for the forward sweeping. This deviation is mostly attributed to the existence of the negative bias stress effect because the effect has not been included in the current model. More thorough investigation is needed to further fine-tune the model in the future.

On the other hand, carrier mobility is another important performance parameter of the transistor. However, when the hysteresis phenomenon exists, the determination of mobility becomes difficult because there are two separate transfer curves, associated with forward and backward sweepings, with different mobility values derived from the transconductance. Because the coefficient α has a strong influence on the transfer curve, the effect of α on the mobility is worth being explicitly discussed. Figure 5a shows the peak mobility obtained from the simulated transfer curves of the device. For a fair and consistent comparison, the peak mobility used in the model is given as well. As can be seen, the simulated mobility value is always overestimated, exhibiting an increasing trend with the increasing α value due to the fact that α is an attenuation coefficient in the forward sweeping. In addition, the peak mobility without any hysteresis (i.e., no charge traps) is also shown as a dashed line in Figure 5a. This mobility value is determined to be 889 $cm^2\ V^{-1}\ s^{-1}$, which is larger than the peak mobility in the model (568 $cm^2\ V^{-1}\ s^{-1}$) and the largest peak mobility in the simulation (880 $cm^2\ V^{-1}\ s^{-1}$ for α = 1 for both forward and backward sweepings). Technically, using transconductance to determine the gate voltage-dependent carrier mobility of the transistor is not valid because eq 1 has a basic assumption that the mobility is independent of gate voltage, although this method has been widely adopted in the literature.[8,33,35,36] The overestimation of the mobility without considering the existence of charge traps is mainly caused by the misuse of transconductance to determine the carrier mobility. Similarly, the smaller peak mobility derived from the simulated transfer curve is attributed to the existence of charge

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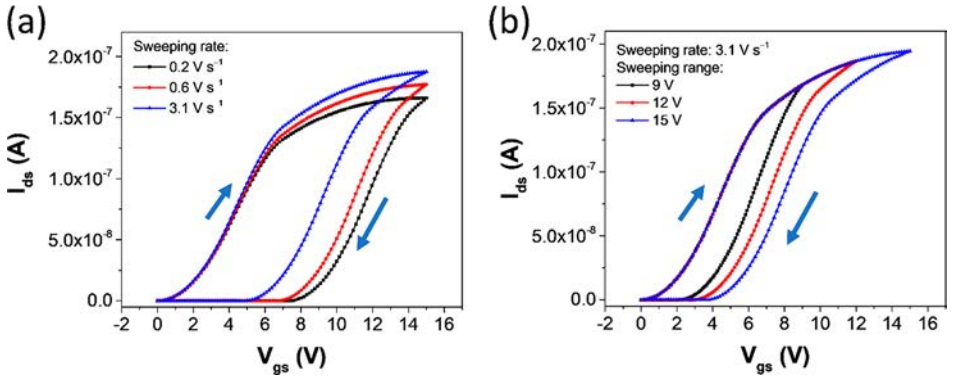

Figure 4. Simulation results for the transfer characteristics of the InAs nanowire FET. (a) Transfer curves at different sweeping rates. The values of α are set to 0.795, 0.795, and 0.82 when the sweeping rates are 0.2, 0.6, and 3.1 V s^{-1}, respectively, for the forward sweeping. The values of α are set to 1.34, 1.34, and 1.19 when the sweeping rates are 0.2, 0.6, and 3.1 V s^{-1}, respectively, for the backward sweeping. (b) Transfer curves at different sweeping ranges. The values of α are set to 0.85 and 1.1, respectively, for forward and backward sweepings. In the simulation, the diameter of the InAs nanowire is 30 nm, the SiO_2 dielectric is 50 nm, and the V_{ds} is 20 mV.

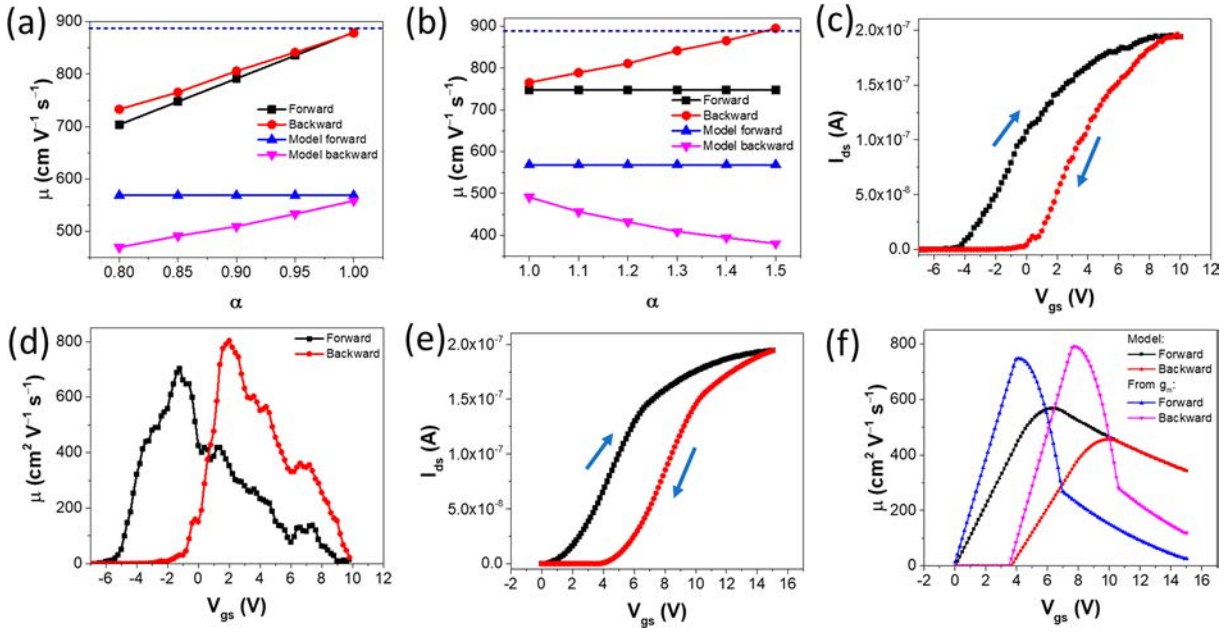

Figure 5. Simulated and measured mobility and transfer characteristics of the InAs nanowire FET. (a) Mobility as a function of different α values for the simulation in the forward sweeping. The α value is kept at 1 for the backward sweeping. (b) Mobility as a function of different α values for the simulation in the backward sweeping. The α value is kept at 0.85 in the forward sweeping. The dashed lines in (a) and (b) show the mobilities determined from the simulated transfer curves without any hysteresis. (c) Measured transfer curves of the NW device. (d) Mobility derived from the measured transfer curves. (e) Simulated transfer curves of the NW device. (f) Mobility model utilized in the simulation and mobility derived from simulated transfer curves. Sweeping rate is set to 3.1 V s^{-1}, and V_{ds} is set to 20 mV. In the simulation, the α values are set to 0.85 and 1.1 for the forward and backward sweepings, respectively.

trapping. It is also noted that the peak mobility value extracted from the backward sweeping is larger than that of the forward sweeping, which is associated with the introduction of α with a value <1. When the α value is fixed at 0.85 for the forward sweeping with only the α value changing in the backward sweeping, the peak mobility value can also be affected. With the increasing α in the backward sweeping, the peak mobility is observed to increase accordingly, whereas the peak mobility remains constant for the forward sweeping (Figure 5b). This unchanged peak mobility is due to the unchanged attenuation coefficient in the forward sweeping. The increase of peak mobility extracted from the backward sweeping is caused by the enhanced depletion of carriers in the channel. Next, the model used in the simulation is further investigated to fit the experimental data. Figure 5c shows the typical transfer curves of the NW FET with hysteresis, while Figure 5d depicts the corresponding mobility determined from the transconductance as a function of gate voltage. Evidently, the forward peak mobility is smaller than the backward peak mobility, being consistent with the simulation results discussed earlier. To have a good match with the experimental data, the α values are determined to be 0.85 and 1.1 for the forward and backward sweepings, respectively (see Figure S6 for the details). Although the determination of α is somewhat arbitrary because the final curves are related to many parameters, the obtained result can also reveal the important underlying physics here. For example, parts e and f of Figure 5 demonstrate the simulated results. It is seen that the hysteresis

https://dx.doi.org/10.1021/acsami.0c17317
ACS Appl. Mater. Interfaces 2020, 12, 56330−56337

loop is almost the same as the experimental result except for the threshold voltage position, as the threshold voltage is set to 0 in the forward sweeping for simplicity. The simulated peak mobility values for forward and backward sweepings are found to be 746 and 793 $cm^2\ V^{-1}\ s^{-1}$, respectively, which is consistent with the experimental findings (forward, 706 $cm^2\ V^{-1}\ s^{-1}$; backward, 807 $cm^2\ V^{-1}\ s^{-1}$). Obviously, the peak mobility values obtained in the simulation and experiment are larger than the peak mobility in the model (568 $cm^2\ V^{-1}\ s^{-1}$), indicating that the peak mobility is indeed overestimated. Because the NW mobility cannot be modeled by a simple formula, importantly being different for different NWs, it is difficult to accurately determine the actual mobility of the NW. Further investigations are needed to explore a further understanding of the transport behavior in NW-based FETs.

CONCLUSION

In summary, we have investigated thoroughly the gate bias stress instability and hysteresis effects in InAs nanowire-based FETs. It is found that the gate bias stress would lead to the shift of threshold voltage and the change of output current. The gate bias stress effect also gets enhanced when the bias stress time is prolonged. At the same time, the hysteresis behavior depends heavily on the gate sweeping rate. A slow sweeping would lead to the large hysteresis. More importantly, during the device operation, the trapped electrons are observed to play a dominant role in the gate bias stress instability and hysteresis effects. The hysteresis behavior can be reproduced by combining the rate equation model and the empirical model to simulate the electron trapping process and the variation of carrier mobility as a function of gate voltage, respectively. Furthermore, the peak mobility derived from the trans-conductance is confirmed to be always overestimated with a larger value in the backward sweeping. All these findings not only offer a simple but effective way to evaluate the fundamental characteristics of charge traps but also provide valuable insights into device performance enhancement for the nanowire-based FETs.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.0c17317.

> Statistical data of the mobility; gate voltage bias stress and hysteresis effects of additional devices; determination process of the output current; time dependent on the current; schematic of the mobility determination; and comparison of transfer curves between experimental and simulation results (PDF)

AUTHOR INFORMATION

Corresponding Author

Johnny C. Ho − *Department of Materials Science and Engineering and State Key Laboratory of Terahertz and Millimeter Waves, City University of Hong Kong, Kowloon 999077, Hong Kong SAR; Key Laboratory of Advanced Materials Processing & Mold (Zhengzhou University), Ministry of Education, Zhengzhou 450002, P. R. China;* orcid.org/0000-0003-3000-8794; Email: johnnyho@cityu.edu.hk

Authors

Changyong Lan − *State Key Laboratory of Electronic Thin Films and Integrated Devices, and School of Optoelectronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 610054, P. R. China;* orcid.org/0000-0002-5654-1098

SenPo Yip − *Department of Materials Science and Engineering and State Key Laboratory of Terahertz and Millimeter Waves, City University of Hong Kong, Kowloon 999077, Hong Kong SAR*

Xiaolin Kang − *Department of Materials Science and Engineering, City University of Hong Kong, Kowloon 999077, Hong Kong SAR*

You Meng − *Department of Materials Science and Engineering, City University of Hong Kong, Kowloon 999077, Hong Kong SAR*

Xiuming Bu − *Department of Materials Science and Engineering, City University of Hong Kong, Kowloon 999077, Hong Kong SAR;* orcid.org/0000-0002-2372-2271

Complete contact information is available at: https://pubs.acs.org/10.1021/acsami.0c17317

Author Contributions

$^{\perp}$C.L. and S.P.Y. contributed equally to this work.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This research was financially supported by the General Research Fund (CityU 11211317) and the Theme-based Research (T42-103/16-N) of the Research Grants Council of Hong Kong SAR, China, the National Natural Science Foundation of China (51672229, 61605024, 61775031, and 62074024), Fundamental Research Funds for the Central Universities (ZYGX2018J056), and UESTC Foundation for the Academic Newcomers Award.

REFERENCES

(1) Eaton, S. W.; Fu, A.; Wong, A. B.; Ning, C.-Z.; Yang, P. Semiconductor Nanowire Lasers. *Nature Reviews Materials* **2016**, *1* (6), 16028.

(2) Goktas, N.; Wilson, P.; Ghukasyan, A.; Wagner, D.; McNamee, S.; LaPierre, R. Nanowires for Energy: A Review. *Appl. Phys. Rev.* **2018**, *5* (4), 041305.

(3) Jia, C.; Lin, Z.; Huang, Y.; Duan, X. Nanowire Electronics: From Nanoscale to Macroscale. *Chem. Rev.* **2019**, *119* (15), 9074−9135.

(4) Weber, W. M.; Mikolajick, T. Silicon and Germanium Nanowire Electronics: Physics of Conventional and Unconventional Transistors. *Rep. Prog. Phys.* **2017**, *80* (6), 066502.

(5) Fang, M.; Han, N.; Wang, F.; Yang, Z.-x.; Yip, S.; Dong, G.; Hou, J. J.; Chueh, Y.; Ho, J. C. III−V Nanowires: Synthesis, Property Manipulations, and Device Applications. *J. Nanomater.* **2014**, *2014*, 702859.

(6) Yip, S. P.; Shen, L.; Ho, J. Recent Advances in III-Sb Nanowires: From Synthesis to Applications. *Nanotechnology* **2019**, *30*, 202003.

(7) Zhang, C.; Li, X. III−V Nanowire Transistors for Low-Power Logic Applications: A Review and Outlook. *IEEE Trans. Electron Devices* **2016**, *63* (1), 223−234.

(8) Ford, A. C.; Ho, J. C.; Chueh, Y.-L.; Tseng, Y.-C.; Fan, Z.; Guo, J.; Bokor, J.; Javey, A. Diameter-Dependent Electron Mobility of InAs Nanowires. *Nano Lett.* **2009**, *9* (1), 360−365.

(9) Schroer, M.; Petta, J. R. Correlating the Nanostructure and Electronic Properties of InAs Nanowires. *Nano Lett.* **2010**, *10* (5), 1618−1622.

(10) Bryllert, T.; Wernersson, L.-E.; Froberg, L.; Samuelson, L. Vertical High-Mobility Wrap-Gated InAs Nanowire Transistor. *IEEE Electron Device Lett.* **2006**, *27* (5), 323−325.
(11) Dayeh, S. A.; Aplin, D. P.; Zhou, X.; Yu, P. K.; Yu, E. T.; Wang, D. High Electron Mobility InAs Nanowire Field-Effect Transistors. *Small* **2007**, *3* (2), 326−332.
(12) Johansson, S.; Memisevic, E.; Wernersson, L.-E.; Lind, E. High-Frequency Gate-All-Around Vertical InAs Nanowire MOSFETs on Si Substrates. *IEEE Electron Device Lett.* **2014**, *35* (5), 518−520.
(13) Jie, J.; Zhang, W.; Peng, K.; Yuan, G.; Lee, C. S.; Lee, S. T. Surface-Dominated Transport Properties of Silicon Nanowires. *Adv. Funct. Mater.* **2008**, *18* (20), 3251−3257.
(14) Zhang, S.; Hemesath, E. R.; Perea, D. E.; Wijaya, E.; Lensch-Falk, J. L.; Lauhon, L. J. Relative Influence of Surface States and Bulk Impurities on the Electrical Properties of Ge Nanowires. *Nano Lett.* **2009**, *9* (9), 3268−3274.
(15) Alexander-Webber, J. A.; Groschner, C. K.; Sagade, A. A.; Tainter, G.; Gonzalez-Zalba, M. F.; Di Pietro, R.; Wong-Leung, J.; Tan, H. H.; Jagadish, C.; Hofmann, S.; et al. Engineering the Photoresponse of InAs Nanowires. *ACS Appl. Mater. Interfaces* **2017**, *9* (50), 43993−44000.
(16) Fang, H.; Hu, W.; Wang, P.; Guo, N.; Luo, W.; Zheng, D.; Gong, F.; Luo, M.; Tian, H.; Zhang, X.; et al. Visible Light-Assisted High-Performance Mid-Infrared Photodetectors Based on Single InAs Nanowire. *Nano Lett.* **2016**, *16* (10), 6416−6424.
(17) Wang, F.; Yip, S.; Han, N.; Fok, K.; Lin, H.; Hou, J. J.; Dong, G.; Hung, T.; Chan, K.; Ho, J. C. Surface Roughness Induced Electron Mobility Degradation in InAs Nanowires. *Nanotechnology* **2013**, *24* (37), 375202.
(18) Cheung, H.-Y.; Yip, S.; Han, N.; Dong, G.; Fang, M.; Yang, Z.-x.; Wang, F.; Lin, H.; Wong, C.-Y.; Ho, J. C. Modulating Electrical Properties of InAs Nanowires via Molecular Monolayers. *ACS Nano* **2015**, *9* (7), 7545−7552.
(19) Tsui, D. á. Observation of Surface Bound State and Two-Dimensional Energy Band by Electron Tunneling. *Phys. Rev. Lett.* **1970**, *24* (7), 303.
(20) Choe, M.; Park, W.; Kang, J.-W.; Jeong, S.; Hong, W.-K.; Lee, B. H.; Park, S.-J.; Lee, T. Investigation of Threshold Voltage Instability Induced by Gate Bias Stress in ZnO Nanowire Field Effect Transistors. *Nanotechnology* **2012**, *23* (48), 485201.
(21) Ju, S.; Janes, D. B.; Lu, G.; Facchetti, A.; Marks, T. J. Effects of Bias Stress on ZnO Nanowire Field-Effect Transistors Fabricated With Organic Gate Nanodielectrics. *Appl. Phys. Lett.* **2006**, *89* (19), 193506.
(22) Yang, Z.-x.; Yip, S.; Li, D.; Han, N.; Dong, G.; Liang, X.; Shu, L.; Hung, T. F.; Mo, X.; Ho, J. C. Approaching the Hole Mobility Limit of GaSb Nanowires. *ACS Nano* **2015**, *9* (9), 9268−9275.
(23) Yang, Z.-x.; Han, N.; Fang, M.; Lin, H.; Cheung, H.-Y.; Yip, S.; Wang, E.-J.; Hung, T.; Wong, C.-Y.; Ho, J. C. Surfactant-Assisted Chemical Vapour Deposition of High-Performance Small-Diameter GaSb Nanowires. *Nat. Commun.* **2014**, *5* (1), 5249.
(24) Li, D.; Lan, C.; Manikandan, A.; Yip, S.; Zhou, Z.; Liang, X.; Shu, L.; Chueh, Y.-L.; Han, N.; Ho, J. C. Ultra-Fast Photodetectors Based on High-Mobility Indium Gallium Antimonide Nanowires. *Nat. Commun.* **2019**, *10* (1), 1664.
(25) Zhou, Z.; Lan, C.; Yip, S.; Wei, R.; Li, D.; Shu, L.; Ho, J. C. Towards High-Mobility $In_{2x}Ga_{2-2x}O_3$ Nanowire Field-Effect Transistors. *Nano Res.* **2018**, *11* (11), 5935−5945.
(26) Dayeh, S. A.; Susac, D.; Kavanagh, K. L.; Yu, E. T.; Wang, D. Field Dependent Transport Properties in InAs Nanowire Field Effect Transistors. *Nano Lett.* **2008**, *8* (10), 3114−3119.
(27) Guo, N.; Hu, W.; Liao, L.; Yip, S.; Ho, J. C.; Miao, J.; Zhang, Z.; Zou, J.; Jiang, T.; Wu, S.; et al. Anomalous and Highly Efficient InAs Nanowire Phototransistors Based on Majority Carrier Transport at Room Temperature. *Adv. Mater.* **2014**, *26* (48), 8203−8209.
(28) Lynall, D.; Nair, S. V.; Gutstein, D.; Shik, A.; Savelyev, I. G.; Blumin, M.; Ruda, H. E. Surface State Dynamics Dictating Transport in InAs Nanowires. *Nano Lett.* **2018**, *18* (2), 1387−1395.
(29) Shen, L.-F.; Yip, S.; Yang, Z.-x.; Fang, M.; Hung, T.; Pun, E. Y.; Ho, J. C. High-Performance Wrap-Gated InGaAs Nanowire Field-Effect Transistors with Sputtered Dielectrics. *Sci. Rep.* **2015**, *5*, 16871.
(30) Bube, R. H. *Photoelectronic Properties of Semiconductors*; Cambridge University Press: New York, 1992.
(31) Fang, H.; Hu, W. Photogating in Low Dimensional Photodetectors. *Advanced Science* **2017**, *4* (12), 1700323.
(32) Zhang, K.; Peng, M.; Yu, A.; Fan, Y.; Zhai, J.; Wang, Z. L. A Substrate-Enhanced MoS_2 Photodetector Through A Dual-Photogating Effect. *Mater. Horiz.* **2019**, *6* (4), 826−833.
(33) Dayeh, S. A.; Yu, E. T.; Wang, D. Transport Coefficients of InAs Nanowires as A Function of Diameter. *Small* **2009**, *5* (1), 77−81.
(34) He, Z.; Zhang, W.; Zhang, W.; Jie, J.; Luo, L.; Yuan, G.; Wang, J.; Wu, C. M. L.; Bello, I.; Lee, C.-S.; et al. High-Performance CdSe: In Nanowire Field-Effect Transistors Based on Top-Gate Configuration with High-K Non-Oxide Dielectrics. *J. Phys. Chem. C* **2010**, *114* (10), 4663−4668.
(35) Liu, H.; Peng, R.; Chu, S.; Chu, S. High Mobility ZnO Nanowires for Terahertz Detection Applications. *Appl. Phys. Lett.* **2014**, *105* (4), 043507.
(36) Cha, S.; Jang, J.; Choi, Y.; Amaratunga, G.; Ho, G.; Welland, M.; Hasko, D.; Kang, D.-J.; Kim, J. High Performance ZnO Nanowire Field Effect Transistor Using Self-Aligned Nanogap Gate Electrodes. *Appl. Phys. Lett.* **2006**, *89* (26), 263102.

https://dx.doi.org/10.1021/acsami.0c17317
ACS Appl. Mater. Interfaces 2020, 12, 56330−56337