Area-Selective Atomic Layer Deposition: Conformal Coating, Subnanometer Thickness Control, and Smart Positioning

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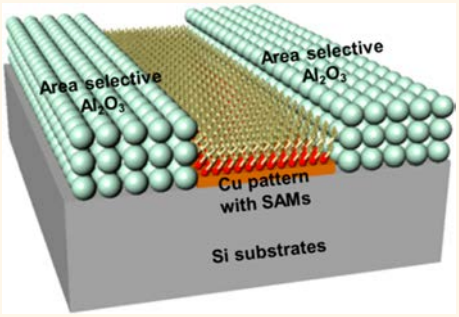
ABSTRACT Transistors have already been made three-dimensional (3D), with device channels (*i.e.*, fins in trigate field-effect transistor (FinFET) technology) that are taller, thinner, and closer together in order to enhance device performance and lower active power consumption. As device scaling continues, these transistors will require more advanced, fabrication-enabling technologies for the conformal deposition of high-κ dielectric layers on their 3D channels with accurate position alignment and thickness control down to the subnanometer scale. Among many competing techniques, area-selective atomic layer deposition (AS-ALD) is a promising method that is well suited to the requirements without the use of complicated, complementary metal-oxide semiconductor (CMOS)-incompatible processes. However, further progress is limited by poor area selectivity for thicker films formed *via* a higher number of ALD cycles as well as the prolonged processing time. In this issue of *ACS Nano*, Professor Stacy Bent and her research group demonstrate a straightforward self-correcting ALD approach, combining selective deposition with a postprocess mild chemical etching, which enables selective deposition of dielectric films with thicknesses and processing times at least 10 times larger and 48 times shorter, respectively, than those obtained by conventional AS-ALD processes. These advances present an important technological breakthrough that may drive the AS-ALD technique a step closer toward industrial applications in electronics, catalysis, and photonics, *etc.* where more efficient device fabrication processes are needed.



In the past few decades, semiconductor technology improvements have been extensively driven by electronic device scaling. Since the high-κ/metal gate device configuration was adopted for the Si transistor design by Intel in 2007, atomic layer deposition (ALD) has become one of the enabling fabrication techniques to push device performance and energy efficiency forward.[1,2] Currently, transistors are departing from conventional planar structures and are moving into three dimensions with the current flowing on three sides of the device channel (*i.e.*, top, left, and right in the 22 nm trigate FinFET technology); the advances of ALD achieving pinhole-free high-κ films over 3D channels has been critical for this development.[3] Unlike the conventional gate dielectric of SiO_2, which can be grown on Si by thermal oxidization, ALD is a deposition scheme that enables the conformal coating of dielectric films with subnanometer control in thickness from vapor sources.[4,5] In contrast to standard physical and/or chemical vapor depositions, an ALD process is implemented by alternating pulses of gaseous chemical precursors that react with the substrate.[5] During each exposure, surface reactions occur only at the reactive sites, which restrict the formation of films to one atomic layer at a time. This self-limiting nature of surface reactions minimizes the influences of any uncontrollable parameters (*e.g.*, randomness of the precursor flux) during film coating because extra precursors are removed and evacuated after each pulse. As a result, the deposited ALD films are atomically smooth and conformal to the substrate, even with high aspect ratio nanostructures and, thus,

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perfect for use in high-quality dielectrics for continued device miniaturization.

During the ALD process, film nucleation is highly dependent on the surface chemistry of the substrate. It is possible to achieve area-selective atomic layer deposition (AS-ALD) by chemically tailoring the substrate surface. Since AS-ALD can offer a number of advantages in transistor fabrication, including reduction of the lithography steps required, elimination of complicated etching processes, and minimization of expensive and poisonous reagent use, the possibility of performing highly efficient AS-ALD has been widely pursued in recent years. In most cases, self-assembled monolayers (SAMs) are utilized as the resist layer for ALD by converting the chemically reactive sites on substrates into their nonreactive forms. For instance, alkylsilanes have been utilized as surface modifiers on silicon to block ALD nucleation for area-selective deposition of a variety of inorganic films such as ZnO, TiO_2, HfO_2, and ZrO_2.[6−8] Octadecylphosphonic acid (ODPA) has also been used to form well-packed resist layers on patterned metal surfaces so that ALD layers can be selectively deposited only on the metal-free regions.[9−11] To achieve a successful AS-ALD, the SAM blocking layers should be defect-free to eliminate the undesired growth of depositing materials on the passivated region. Unfortunately, preparing a defect-free SAM is extremely difficult and generally requires a prolonged deposition time, which is typically more than 48 h.[7,10] Moreover, even with a high-quality SAM resist layer, the selectivity may still be limited to only a few nanometers of the ALD films. These problems may serve to undermine the competence of AS-ALD as a simple and inexpensive process that deserves to be adopted in industrial productions.

Atomic layer deposition is a deposition scheme that enables the conformal coating of dielectric films with subnanometer control in thickness from vapor sources.

In this issue of *ACS Nano*, Bent and co-workers,[11] one of the pioneering research teams with expertise in a wide variety of ALD schemes, report a self-correcting process that allows the selective deposition of dielectric films with thickness at least 10 times larger than those obtained by conventional AS-ALD processes. This self-correcting method is, in principle, achieved by combining a selective deposition process with a mild chemical etching step, as illustrated in Figure 1. By employing the intrinsically selective adsorption of ODPA on Cu, the authors created a resist layer only on the surface of Cu that prepatterned on the silicon substrate. They then performed ALD over the patterns to deposit thin Al_2O_3 films predominately on the Si surface, with only small amounts growing on the Cu regions. At the same time, the selectivity was further increased by coupling with a gentle chemical etching step after deposition, and as a result, thick films (up to 550 deposition cycles) can be patterned with perfect position alignment. In a previous study by the Bent's research group, an electrochemical method was implemented to remove SAMs from oxidized copper in order to increase the selectivity for molecular layer deposition and ALD films;[10] however, such a method might not be compatible with many electronic device fabrication processes. In the present work, they employ a wet chemical etching process to remove the SAMs and the undesired ALD coatings selectively. In particular, they use acetic acid, a mild etchant that does not harm the ALD film on silicon but is still strong enough for SAM removal through selective etching of the underlying native oxide layer on Cu. In addition to the enhanced selectivity, another notable advantage of this combined AS-ALD/chemical etching approach is that it can greatly save time on SAM preparation, because it is no longer necessary to ensure that the SAM is defect-free. As shown in Figure 2, with a post-ALD chemical etching process, ODPA SAMs deposited for 1 h are already robust enough for the selective deposition of Al_2O_3 with a maximum achievable thickness up to 550 cycles and a minimum feature size down to 500 nm on Cu/Si patterns.

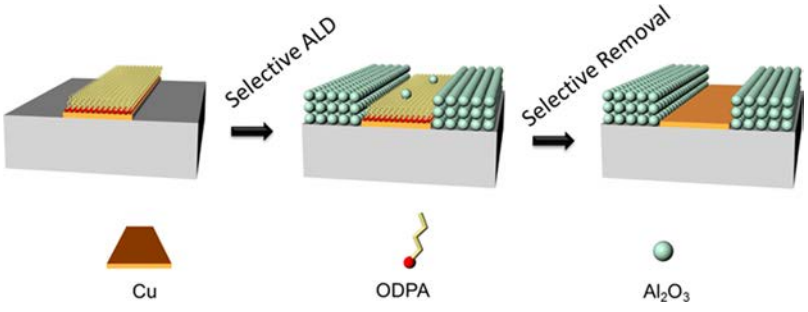

Figure 1. Illustrative schematic demonstrating the hybird AS-ALD process, which combines the selective deposition and selective removal steps.

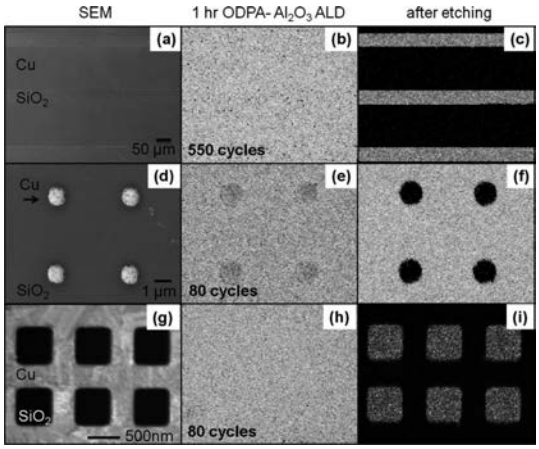

Figure 2. SEM images of Cu/SiO_2 patterns subjected to 1 h of ODPA exposure followed by Al_2O_3 ALD and acetic acid sonication. Reproduced from ref 11. Copyright 2015 American Chemical Society.

OUTLOOK AND FUTURE CHALLENGES

Currently, ALD plays an important role in electronics industries by providing high-quality and conformal high-k gate dielectrics for the fabrication of transistors. As device scaling continues, second-generation 3D trigate transistors will be made with 14 nm technology with fins (*i.e.*, device channel) that are made taller, thinner, and closer together, enabling higher performance and less active power consumption.[12] Regardless, these fins with their higher aspect ratios protruding from the surface make lithography of dielectric regions far more challenging. One feasible solution may be the adoption of this newly developed AS-ALD scheme, which can pattern dielectrics with superior atomic control in both thickness and lateral dimensions. Note that since SAMs are utilized as blocking resists for ALD, the method described by Bent *et al.* may facilitate easy integration with monolayer doping (MLD),[13] another SAM-based next-generation doping technology now listed in the fabrication roadmap,[14] in order to simplify the complexity of future device fabrication but still obtain a much higher yield.

Another important aspect that must be evaluated in the near future is the validity of the selectivity of these AS-ALD processes for the downscaling of feature sizes. Although

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Bent *et al.* demonstrated the patternable feature size in the range from several tens of micrometers all the way down to a few hundred of nanometers,[11] this feature size is still too large and not comparable to state-of-the-art device dimensions; further exploration is needed and warranted in this direction. Moreover, the process compatibility of AS-ALD with other fabrication steps also requires further assessment. The post-ALD etching process may have harmful effects on the functional components of commercial device chips. For example, future integrated circuit devices may resort to using alternative channel materials, such as III–V compounds and Ge for the continued reduction of power consumption and the enhancement of transition speeds; however, some of these materials are vulnerable to the acids used for SAM removal. More importantly, although excellent area selectivity has been achieved in this self-correction approach, it mostly relies on the use of copper patterns, which may induce additional transistor integration complexity similar to the ones in dual-Damascene processes;[15] alternative underlying metal layers may be needed for this AS-ALD scheme.

Along with electronics applications, AS-ALD may also find potential practical application in other technological domains such as hybrid catalysts, photonic crystals, and optoelectronic devices, which require conformal coating of dielectrics and metals over large areas with superior control in film thickness, tunable feature size, and excellent position alignment.[16–19] One example is that AS-ALD of Pt patterns have been successfully attained and demonstrated to be efficient electrode catalysts and current collectors for high-performance solid oxide fuel cells with enhanced power density.[5,17] For these other applications, the processing methods of AS-ALD can be modified accordingly to address different requirements.

Conflict of Interest: The authors declare no competing financial interest.

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