ACSNANO
www.acsnano.org
ARTICLE

Complementary Metal Oxide Semiconductor-Compatible, High-Mobility, ⟨111⟩-Oriented GaSb Nanowires Enabled by Vapor–Solid–Solid Chemical Vapor Deposition

Zai-xing Yang,[†,‡] Lizhe Liu,[§] SenPo Yip,[‡,∥] Dapan Li,[‡] Lifan Shen,[∥,⊥] Ziyao Zhou,[‡] Ning Han,[*,#] Tak Fu Hung,[‡] Edwin Yue-Bun Pun,[∥,⊥] Xinglong Wu,[§] Aimin Song,[†,▽] and Johnny C. Ho[*,‡,∥]

[†]Center of Nanoelectronics and School of Microelectronics, Shandong University, Jinan 250100, PR China

[‡]Department of Physics and Materials Science and [⊥]Department of Electronic Engineering, City University of Hong Kong, 83 Tat Chee Avenue, Kowloon, Hong Kong

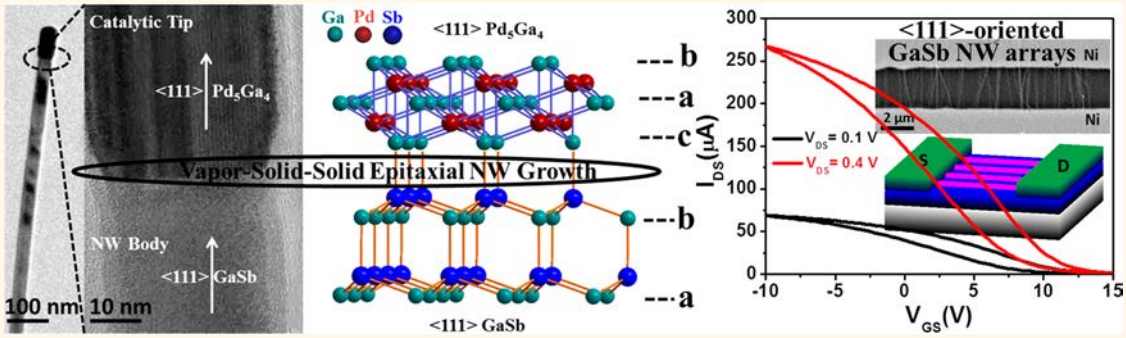
[§]Key Laboratory of Modern Acoustics, MOE, Institute of Acoustics, Collaborative Innovation Center of Advanced Microstructures, National Laboratory of Solid State Microstructures, Nanjing University, Nanjing 210093, PR China

[∥]State Key Laboratory of Millimeter Waves, City University of Hong Kong, 83 Tat Chee Avenue, Kowloon, Hong Kong

[#]State Key Laboratory of Multiphase Complex Systems, Institute of Process Engineering, Chinese Academy of Sciences, Beijing 100190, PR China

[▽]School of Electrical and Electronic Engineering, University of Manchester, Manchester M13 9PL, U.K.

Supporting Information



ABSTRACT: Using CMOS-compatible Pd catalysts, we demonstrated the formation of high-mobility ⟨111⟩-oriented GaSb nanowires (NWs) *via* vapor–solid–solid (VSS) growth by surfactant-assisted chemical vapor deposition through a complementary experimental and theoretical approach. In contrast to NWs formed by the conventional vapor–liquid–solid (VLS) mechanism, cylindrical-shaped Pd_5Ga_4 catalytic seeds were present in our Pd-catalyzed VSS-NWs. As solid catalysts, stoichiometric Pd_5Ga_4 was found to have the lowest crystal surface energy and thus giving rise to a minimal surface diffusion as well as an optimal in-plane interface orientation at the seed/NW interface for efficient epitaxial NW nucleation. These VSS characteristics led to the growth of slender NWs with diameters down to 26.9 ± 3.5 nm. Over 95% high crystalline quality NWs were grown in ⟨111⟩ orientation for a wide diameter range of between 10 and 70 nm. Back-gated field-effect transistors (FETs) fabricated using the Pd-catalyzed GaSb NWs exhibit a superior peak hole mobility of ~330 $cm^2 V^{-1} s^{-1}$, close to the mobility limit for a NW channel diameter of ~30 nm with a free carrier concentration of ~10^{18} cm^{-3}. This suggests that the NWs have excellent homogeneity in phase purity, growth orientation, surface morphology and electrical characteristics. Contact printing process was also used to fabricate large-scale assembly of Pd-catalyzed GaSb NW parallel arrays, confirming the potential constructions and applications of these high-performance electronic devices.

KEYWORDS: *GaSb nanowires, growth orientation, high mobility, vapor–solid–solid, interface plane orientation, in-plane lattice mismatch*

Received: February 21, 2017
Accepted: March 29, 2017
Published: March 29, 2017

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237–4246

Due to their tunable bandgaps, composition, structural configurations and superior carrier mobilities, one-dimensional (1D) III–V semiconductor nanowires (NWs) are widely recognized as promising fundamental building blocks for next-generation electronics, photonics, *etc.*[1−12] In particular, GaSb NWs have drawn a lot of attention recently for many advanced device utilizations since GaSb is a technologically important p-type semiconductor with a band gap of 0.726 eV, a high theoretical hole mobility of up to 1000 $cm^2 V^{-1} s^{-1}$, and an impressively strong spin–orbit interaction.[13−18] Although there remains a substantial challenge to obtain very thin and "nontapered" GaSb NWs owing to the uncontrolled radial growth arising from the Gibbs–Thomson effect, high-quality and uniform GaSb NWs with diameters down to 20 nm have been successfully prepared using a sulfur-surfactant technique, which efficiently stabilizes the high-energy sidewalls for homogeneous NW formation during the chemical vapor deposition (CVD) process.[19,20] However, the growth direction and corresponding carrier mobilities are still found to be heavily dependent on the NW diameters. ⟨111⟩-oriented GaSb NWs exhibit the highest hole mobility because of the optimized surface passivation and roughness resulting in minimized surface traps, thus indicating the potential applications of these phase-pure NWs for high-performance electronics.[20]

In the previously reported surfactant-assisted growth technique, Au was typically utilized as the catalyst for the synthesis of high-quality GaSb NWs with excellent yields *via* vapor–liquid–solid (VLS) mode.[19,20] Unfortunately, Au is notorious for its complementary metal oxide semiconductor (CMOS) incompatibility; hence, the use of Au catalyst may restrict the deployment of these NWs for large-scale semiconductor device integration.[21−24] Therefore, it is crucial to explore alternative means to synthesize CMOS-compatible NWs with well-controlled physical properties. For example, Robertson *et al.* employed the CMOS-compatible catalyst of Pd for the CVD synthesis of Si NWs *via* vapor–solid–solid (VSS) scheme.[25] Although both Au and Pd are transition metals, their behaviors are dramatically different when they diffuse into the Si lattice.[26,27] Once Au diffuses into Si, it forms fatal defects quickly and deteriorates electrical properties of Si, making it CMOS-incompatible.[28] On the other hand, when Pd diffuses into the Si lattice, instead of forming defects, it readily forms palladium silicide (Pd_2Si), a compound commonly employed as an electrical contact of Si devices. As a result, Pd is categorized as CMOS-compatible in the Si community.[21,29] The case of CMOS-compatible catalyst of Ni is similar to Pd, and Ni-catalyzed InAs NWs with electron mobilities up to 10 000 $cm^2 V^{-1} s^{-1}$ have also been successfully synthesized by Javey *et al.* and others.[30,31] However, there are still limited reports of high-performance, uniform, phase-pure and, more importantly, CMOS-compatible GaSb NWs for large-scale practical device applications.

In this work, using a complementary experimental and theoretical approach, we demonstrated the use of the VSS technique to obtain CMOS-compatible, high-mobility, phase-pure ⟨111⟩-oriented GaSb NWs. In contrast to Au-catalyzed GaSb NWs grown with mixed orientations and wide distributions of diameters *via* VLS mode,[19,20] our Pd-catalyzed GaSb NWs obtained were all grown along the ⟨111⟩ direction, with a narrow diameter distribution of 26.9 ± 3.5 nm. As an immobile solid catalysts, stoichiometric Pd_5Ga_4 was found to consist of the lowest crystal surface energy, contributing to the uniform nucleation of catalytic seeds with minimal surface diffusion and optimal seed/NW interface plane relationship. This resulted in s minimal diameter variation and excellent phase purity in the NWs. When these NWs were fabricated into back-gated field-effect transistors (FETs), the typical Pd-catalyzed GaSb NW exhibited a high peak hole mobility of ∼330 $cm^2 V^{-1} s^{-1}$. This mobility value is close to the mobility limit for a 30 nm NW channel diameter with a free carrier concentration of $\sim 10^{18}$ cm^{-3},[32,33] indicating that the NWs have a high phase purity, homogeneous growth orientation, and excellent surface morphology. By using the contact printing process, the versatility of these NWs was further illustrated with the configuration of NW parallel-arrayed transistors with impressive device performances. All these results confirm the promise of these high-performance and CMOS-compatible GaSb NWs for a wide range of future technological applications.

RESULTS AND DISCUSSION

In order to achieve CMOS-compatible GaSb NWs using the sulfur-surfactant assisted CVD technique, various metal catalysts, such as Pd, Ni and Cu, which would form higher temperature eutectoids with Ga, were employed in this work to evaluate the VSS growth mechanism. The NW growths were always maintained at temperatures lower than the catalytic eutectic temperatures to ensure the VSS scheme.[25,34−38] A typical scanning electron microscope (SEM) image of Pd-catalyzed GaSb NWs is shown in Figure 1a, and the SEM images of Ni- and Cu-catalyzed NWs can also be found in Supporting Information Figure S1. Using optimized growth conditions, the Pd catalyst yields GaSb NWs with the most uniform surface morphology and highest growth density among all catalyst choices. In general, Pd-catalyzed NWs are thin and long, up to 35 μm in length (Figure 1a inset). In the case of Au-catalyzed NWs, the length is less than 20 μm for the same growth duration (Supporting Information Figure S2a). Therefore, we found that the growth rate of Pd-catalyzed GaSb NWs (∼100 μm/h) is much faster than the Au-catalyzed NWs (∼60 μm/h). As shown in the TEM image in Figure 1b, the representative NW displays a smooth surface with a cylindrical-shaped catalytic tip and no tapering. This nonspherical tip clearly confirms that the VSS growth mechanism occurred at this location.[37,38] Thin Pd-catalyzed GaSb NWs with a diameter of 17 nm grows along the ⟨111⟩ direction, while Au-catalyzed GaSb NWs in this diameter range always grow along the ⟨211⟩ direction.[20] Hence there is a fundamental difference in the growth mechanism of NWs using Pd and Au catalysts (*i.e.*, VSS *versus* VLS modes). Indeed, although both Pd- and Au-catalyzed NWs are grown with the same zinc-blende (ZB) crystal structure as demonstrated in the XRD patterns (Figure S 2d, JCPDS Card No. 07–0215), Pd-catalyzed NWs are found to have a dominant growth orientation along the ⟨111⟩ direction (*i.e.*, 30 out of 31 NWs) (Figure 1c and Supporting Information Figure S3). This finding is in contrast to that of Au-catalyzed NWs, where there are mixed growth orientations which are diameter dependent, similar to previously reported work.[20,39−41] Moreover, based on more than 100 NWs observed by TEM (Figure S2b and c), Pd-catalyzed NWs (grown by 1 nm catalyst film) have smaller diameters and a much narrower distribution (26.9 ± 3.5 nm) compared with those of Au-catalyzed NWs (42.1 ± 11.7 nm) (Figure 1d). This diameter uniformity is more prominent when thicker catalyst films (*i.e.*, 2 to 8 nm) were used for NWs with larger diameters (Figure S2e). These thinner diameter, narrower distribution and exceptional single-orientation phase-purity GaSb NWs grown using Pd catalysts are suitable for large-scale and high-performance advanced devices.

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237–4246

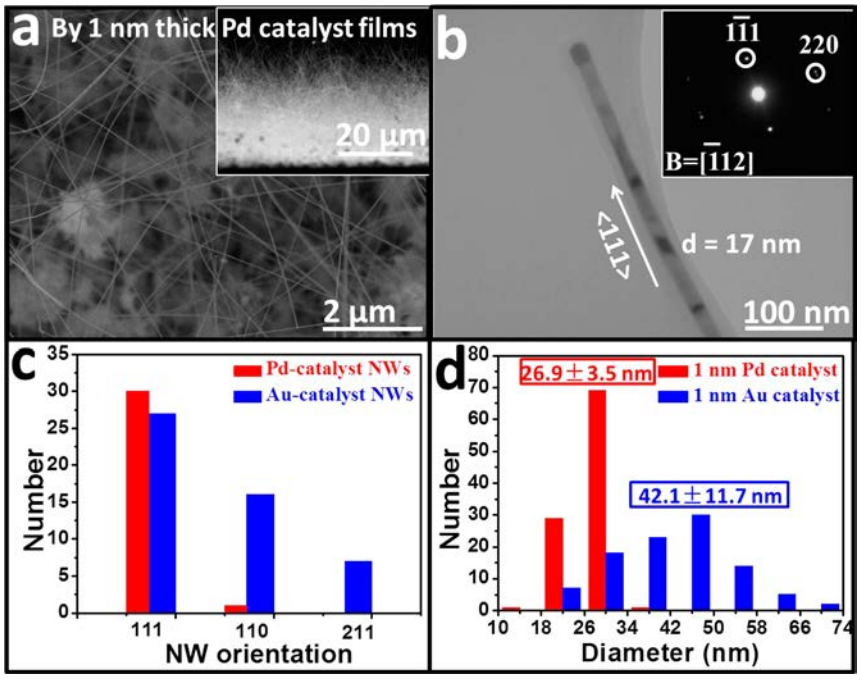


Figure 1. CMOS-compatible catalyst of Pd was used for the GaSb NW growth. (a) SEM image of the GaSb NWs grown by 1 nm Pd catalyst film, inset shows the corresponding cross-sectional SEM image. (b) TEM image of the Pd-catalyzed GaSb NWs with a thin diameter of 17 nm, inset is the corresponding SAED pattern indicating the NW grew along the ⟨111⟩ direction. (c) Growth orientation and (d) Diameter distribution of the NWs grown with 1 nm Pd catalyst film, respectively. Compared with Au-catalyzed GaSb NWs (grown by 1 nm Au film), the Pd-catalyzed NWs show single growth direction and thinner diameter with tighter distribution.

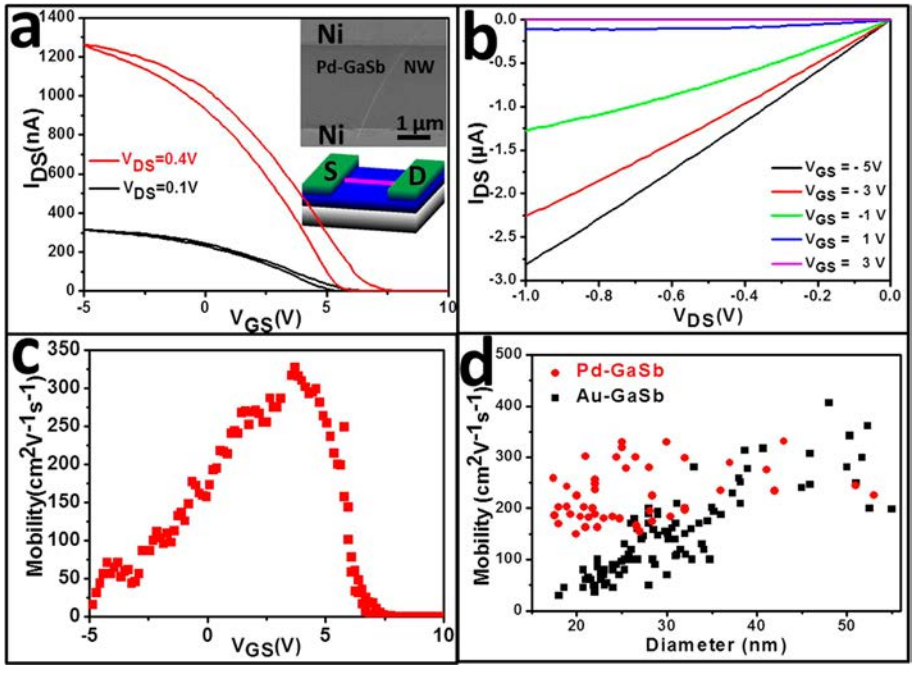


Figure 2. Electrical properties of the Pd-catalyzed GaSb NWs. (a, b) Transfer and output characteristics of the representative VSS grown GaSb NW configured in the back-gated field-effect transistors. The inset (panel a) gives the corresponding SEM image and device schematic of the device fabricated with Ni source/drain contacts. On the basis of the SEM image, the NW diameter, *d*, is found to be 30 nm and the channel length, *L*, is determined to be 3.7 *μ*m. (c) Hole mobility calculation of the NW device. (d) Peak field-effect hole mobility statistics of both Pd- and Au-catalyzed NWs.

Apart from the NW diameter distribution and phase purity, it is also important to assess their corresponding electrical properties of Pd-catalyzed NWs for electronic device utilization. Back-gated NW FETs with channel lengths >2 *μ*m were used to ensure that the diffusive transport of carriers, rather than the ballistic or quasi-ballistic transport, are evaluated, and thus the intrinsic transport property of the NWs such as the carrier mobility can be deduced. As shown in the transfer and output characteristics of a representative NW FET device (Figure 2a and b), a typical p-type conducting behavior with a high ON/OFF

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237−4246

current ratio up to 10^6, as well as an ohmic-like contact formation with Ni source/drain electrodes, is confirmed. The corresponding field-effect hole mobility can be calculated using the well-accepted method based on the square law model.[31] The low-bias (*i.e.*, $V_{DS} = 0.1$ V) transconductance, g_m, can be extracted from the transfer characteristics, $g_m = (dI_{DS})/(dV_{GS})|V_{DS}$ with $\mu = g_m(L^2/C_{ox})(1/V_{DS})$, where C_{ox} is the gate capacitance obtained from the finite element analysis software COMSOL using different NW diameters. The transconductance, g_m, can then be used to calculate the field-effect mobility of an individual NW accurately once the NW channel length and the diameter are known. As given in Figure 2c, the peak hole mobility of the NW is found to be ~330 $cm^2\ V^{-1}\ s^{-1}$, with an estimated hole concentration n_h of ~3.0×10^{18} cm^{-3}. This hole concentration was obtained using the equation $n_h = Q/(q\pi r^2 L) = (C_{ox}V_{th})/(q\pi r^2 L)$, where r is the NW radius (15 nm) and V_{th} is the threshold voltage (~7 V). The I_{ON}/I_{OFF} current ratio and V_{th} can be directly read off from the log-scale and square-root-scale of the transfer curves in Supporting Information Figure S4. When the NW diameters are greater than 40 nm, the peak hole mobility value of the Pd-catalyzed NWs is similar to that of Au-catalyzed NWs, approaching the theoretical mobility limit with a hole concentration of 10^{18} cm^{-3}. However, when the NW diameters are below 40 nm, the ⟨111⟩-oriented Pd-catalyzed thin NWs out-perform their counterparts grown by Au catalysts with mixed ⟨110⟩ and ⟨211⟩ orientations. The mobility values of Pd-catalyzed NWs degrade at a much slower rate as the NW diameter decreases because the phase-pure ⟨111⟩-oriented NWs have minimized surface scattering effect along their atomically smooth {110} surface.[42,43] Because of the negligible diameter dependence of the mobility values, these high-performance, small-diameter and CMOS-compatible GaSb NWs are excellent candidates for device miniaturization.

To shed light on the fundamental mechanistic difference facilitated by Pd catalysts as compared with Au catalysts for the GaSb NW synthesis, the crystallinity, the chemical stoichiometry as well as the growth characteristics of as-grown ⟨111⟩-oriented Pd-catalyzed GaSb NWs are studied using high-resolution TEM (HRTEM) and energy-dispersive X-ray spectroscopy (EDS). Figure 3a shows a representative TEM image of an individual Pd-catalyzed NW, displaying a cylindrical catalytic tip with a length of 70 nm and a diameter of 40 nm. This is different from the spherical shape of NWs using Au catalysts grown in VLS mode. Moreover, as shown in the HRTEM image of catalyst/body region (Figure 3b), both the catalyst tip and NW body grew along the ⟨111⟩ direction and formed a cubic crystal structure. EDS measurements on the composition of the catalyst tip and NW body (Supporting Information Figure S5) show that the cylindrical tip is Pd_5Ga_4 crystal and NW body is stoichiometric GaSb. Also, HRTEM images along the axial direction of the NW, from the catalytic tip to the NW root, shown in Supporting Information Figure S6, display a smooth surface, a uniform ⟨111⟩ growth direction and a diameter of 35 nm throughout the entire NW length (>10 μm long). Furthermore, different cylindrical tip lengths are also observed in HRTEM images (Figure 3c insets). Although the cylindrical tip length changes from ~26 nm to more than 100 nm, they are all oriented in the ⟨111⟩ direction with a stoichiometric Pd_5Ga_4 tip as identified by the HRTEM images (Supporting Information Figure S7) and the EDS spectra. Pd_5Ga_4 crystal is known to have a relatively high eutectic temperature of ~940 °C[44] which is significantly higher than the NW growth temperature of 585 °C employed in this work, thus confirming the VSS growth mode and the presence of

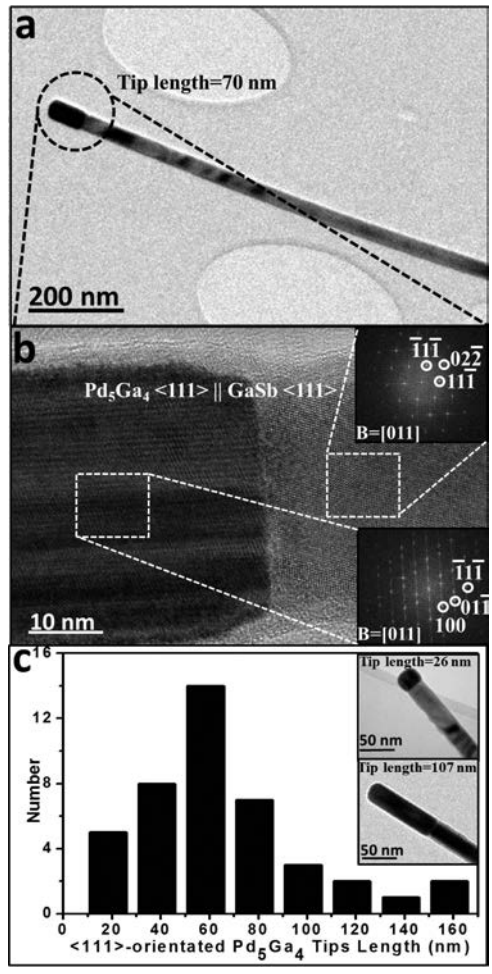


Figure 3. Morphology, crystal structure and tip length statistics of representative Pd-catalyzed GaSb NWs. (a) TEM image of NW with cylindrical catalytic tip. (b) HRTEM image of the catalyst/body region of as-shown NW. Insets show the corresponding FFT images. (c) Pd_5Ga_4 catalyst tip length statistics, insets show the TEM images of NWs with tip lengths of 26 and 107 nm.

nonspherical Pd catalysts. In the CVD process, when the NWs are grown without using any sulfur surfactant, the obtained NWs are severely tapered and coated with surface aggregates, but cylindrical shape catalytic tips still existed (Supporting Information Figure S8). This means that the effect of sulfur surfactant on the nonspherical tips can be excluded while the surfactants are only employed for the *in situ* surface passivation of controlled NW radial growth. In this case, as catalyzed by the ⟨111⟩-oriented Pd_5Ga_4 alloy seeds, all obtained GaSb NWs exhibit excellent crystallinity with uniform ⟨111⟩ growth orientation and without any noticeable amount of crystal defects, such as stacking faults or inversion domains.

The cylindrical catalyst tips are also investigated in details in order to evaluate the comprehensive growth characteristics and their relationship to the obtained superior NW crystal quality, uniform diameter and phase purity. First, the surface energies of Pd_xGa_y catalyst seeds with different compositions and growth orientations are simulated, as shown in Figure 4a and b. The ⟨111⟩-oriented catalyst tip with a Pd:Ga ratio of 5:4 has the lowest surface energy. The surface energy becomes larger for longer tip length, indicating that forming very long catalyst tips is thermodynamically difficult. The surface energies of the solid-state Pd_5Ga_4 crystals (*i.e.*, the catalytic seeds) with different

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237−4246

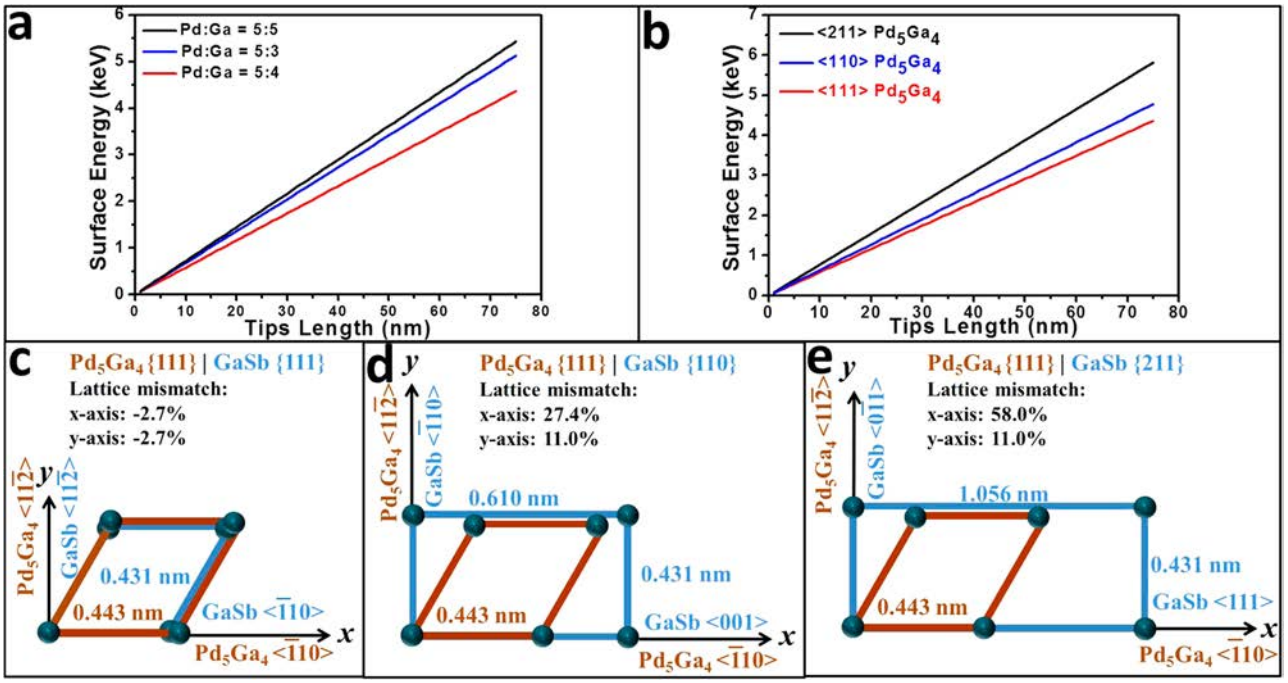


Figure 4. Simulation of catalyst tip surface energy and epitaxy growth model of Pd-catalyzed GaSb NWs. (a) Simulated catalyst tip surface energy as a function of composition. (b) Simulated Pd_5Ga_4 catalyst tip surface energy as a function of growth orientation. (c), (d), (e) Schematic view of the in-plane orientation of catalytic seed/NW interface of Pd_5Ga_4 {111} | GaSb {111}, Pd_5Ga_4 {111} | GaSb {110} and Pd_5Ga_4 {111} | GaSb {211}.

Table 1. Comparison of Surface Energy of Pd_5Ga_4 Catalyst Seed among Different Crystal Planes

Pd_5Ga_4	surface energy (keV)
{001}	1.5322
{110}	1.1492
{111}	1.2582

crystal planes are tabulated in Table 1. The {110} crystal plane has a much lower surface energy than those of {100} and {111}, since the {110} plane has the highest atomic density and thus the lowest surface energy due to the body-centered cubic structure of Pd_5Ga_4 crystal. Since the ⟨111⟩-oriented tips consist of all {110} surface planes[20] with minimal crystal energies and are thermodynamically most favorable, all the observed Pd_5Ga_4 catalytic seeds are oriented in the ⟨111⟩ direction with most of them having a tip length of 60 nm, as shown in Figure 3 and Supporting Information Figure S7.

It is worth pointing out that the surface energy of Pd_5Ga_4 ⟨110⟩ is not that much higher than that of Pd_5Ga_4 ⟨111⟩. However, in the epitaxial NW growth, the lattice mismatch between catalyst tips and NW bodies is also an important consideration which cannot be neglected. Once the ⟨111⟩-oriented Pd_5Ga_4 seeds are obtained, the ⟨111⟩-oriented GaSb NWs are expected to form due to the favorable epitaxial relationship.[45] As depicted in the catalyst seed/NW interface orientation relationship of the cubic Pd_5Ga_4{111}|cubic GaSb{111} in Figure 4c, the atomic arrangement of Ga in the {111} plane of both Pd_5Ga_4 and GaSb crystals exhibit excellent epitaxial characteristics with the smallest in-plane lattice mismatch of 2.7% among all the possible interface configurations. As shown in Supporting Information Figure S9, the in-plane lattice mismatch between Pd_5Ga_4 {110} and GaSb {111} is around 16.1% while the mismatch between Pd_5Ga_4 {110} and GaSb {110} is about 27.4%. As a result, these relatively large lattice mismatches would make the ⟨111⟩-oriented and ⟨110⟩-oriented GaSb NWs difficult to be epitaxially grown from Pd_5Ga_4 ⟨110⟩ tips. The lattice mismatch is calculated using the analytic equation $[(a_{NW} - a_{Cat})/a_{NW} \times 100\%]$, where a_{NW} and a_{Cat} are the lattice constants of the NW and catalyst seeds involved, respectively. The superior lattice matching would enable the obtained GaSb NWs having an enhanced crystal quality and uniform growth orientation, minimizing the probability of NWs grown along other directions such as ⟨110⟩ and ⟨211⟩ with larger lattice mismatch and higher interfacial energy, as schematically shown in Figure 4d and e.

Although WZ GaSb {0001} planes have the same atomic alignment and the same lattice matching with Pd_5Ga_4 {111} planes and ZB GaSb {111} planes, no wurtzite (WZ) ⟨0001⟩-oriented NW has been observed in this study. It is because as shown in the atomic model of the seed/NW interface plane orientation in Figure 5a and b, the difference between the atomic layer stacking sequence in ZB (*i.e.*, "abcabc") and WZ (*i.e.*, "ababab") would make the nucleation of WZ GaSb NWs from the Pd_5Ga_4 seeds not possible. By examining the closely packed plane along both the ZB and the WZ NW growth directions, the first two atomic layer stacking of the ZB and the WZ NW structures are the same, namely "ab"; however, the third atomic layer of the WZ NW structure, namely "a", cannot establish any consistent or stable crystal registration with the catalyst seed located above. Thus, the ⟨111⟩-oriented Pd_5Ga_4 catalytic tip catalyzes predominantly the ZB GaSb NWs growing along the ⟨111⟩ direction with small and uniform diameter under the VSS growth mode, as well as improved crystal quality attributed to the superior in-plane lattice matching at the seed/NW interface.

After investigating the VSS growth mechanism of Pd-catalyzed GaSb NWs, the detailed comparison of the NW growth characteristic between VSS and VLS growth mode is shown

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237−4246

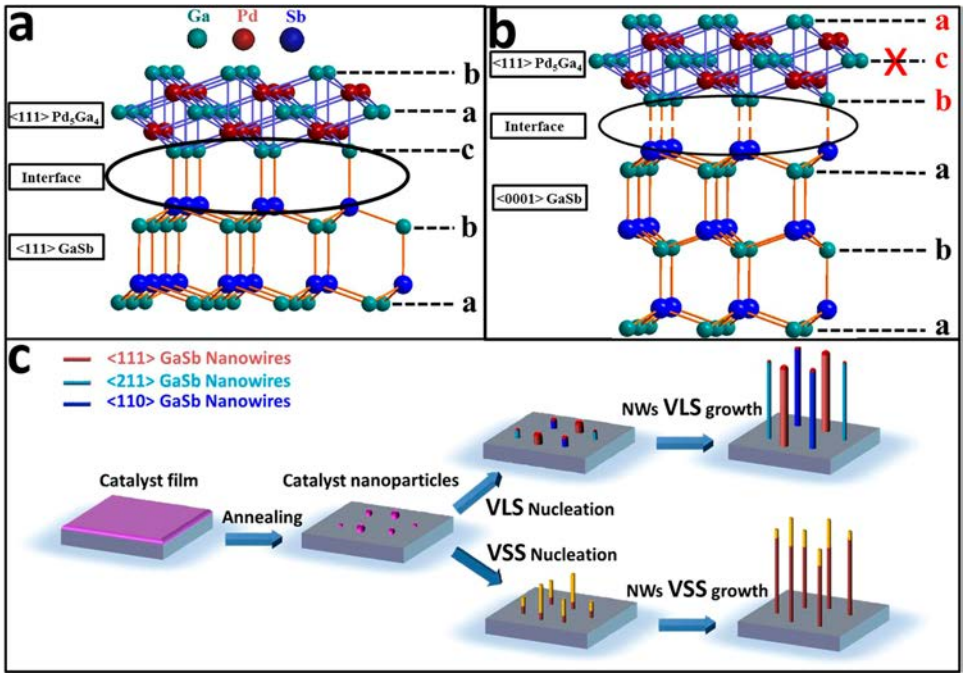


Figure 5. Proposed growth mechanism of Pd-catalyzed GaSb NWs. (a), (b) Approximate atomic models demonstrating the epitaxial relationship between ⟨111⟩-oriented Pd_5Ga_4 seed and ⟨111⟩-oriented GaSb NW, and between ⟨111⟩-oriented Pd_5Ga_4 seed and WZ ⟨0001⟩-oriented GaSb NW. (c) NW growth schematic showing the VLS and VSS growth modes catalyzed by the Au and Pd seeds, respectively.

in Figure 5c. In a typical CVD growth process, the catalyst film will first be annealed at the NW growth temperature, resulting in the formation of nanoscale metal nanoparticles. In the case of NWs grown with Au catalysts, the eutectic temperature of Au−Ga (<500 °C)[46] is lower than the required growth temperature of 545 °C. Hence it is expected that GaSb NWs grow *via* the VLS mode, which is confirmed by the TEM observation of a typical spherical catalytic tip. On the basis of the Gibbs−Thomson effect, these mobile liquid Au_xGa_y nanoparticles would further be aggregated and supersaturated with different precursor compositions, leading to the growth of NWs with different orientations that are determined mainly by the surface energies.[39] In the case of VSS growth mode, the immobile solid catalyst tip is found to grow along close-packed plane with the lowest surface energy, and cylindrical shapes with different lengths are formed. The equivalent spherical diameter can be calculated assuming that the cylinders are transformed into spheres, and after the transformation the Pd catalytic seed has a similar equivalent diameter distribution as that of the Au catalyst (Supporting Information Figure S10). This similar seed diameter distribution is also confirmed by the statistics of the AFM image of the annealed 1 nm thick Pd and Au catalyst, shown in Supporting Information Figure S11. The spherical Pd catalytic seed is first transformed into a cylinder at the initial stage of NW nucleation during the VSS growth mode, leaving only similar circular bottom for the thinner and uniform diameter growth of NWs. Hence, since the seed volume varies in length instead of diameter, it becomes easier to control the NW diameter during the nucleation and the subsequent growth. The crystalline seed dictates the epitaxial growth orientation of NWs *via* the established seed/NW interface plane relationship, which is independent of the NW diameter and growth condition. As a result, compared with a typical VLS-based NW growth mode, the VSS scheme has demonstrated significant advantages in attaining NWs with narrower diameter distributions as well as well-controlled crystal phase and growth orientation.

To further understand the NW growth mechanism, the feasibility of large-scale device integration of the as-prepared CMOS-compatible GaSb NWs is demonstrated with the fabrication of NW parallel-arrayed FETs *via* the well-established NW contact printing technique.[47] The SEM image and device schematic of a typical Pd-catalyzed GaSb NW arrayed FET are shown in Figure 6a. The device channel length and width are designed to be 2.5 and 200 μm, respectively. On the basis of the SEM observation, there are about 400 NWs bridging the source/drain electrodes. As shown in the transfer and output characteristics in Figure 6b and c, the device has a current density of 1.35 μA/μm under V_{DS} = 0.4 V and V_{GS} = −10 V with a p-type conducting behavior and an ohmic-like contact characteristic. The corresponding field-effect mobility against the gate voltage, V_{GS}, is also evaluated and presented in Figure 6d. The mobility is calculated based on the standard square law model similar to the operation of a single NW device. The capacitance is estimated using an upper-bound model that multiplies the capacitance of each nanowire with the number of nanowires in the channel. The calculated peak hole mobility is ~65 $cm^2\ V^{-1}\ s^{-1}$, which is higher than that of state-of-the-art p-type thin-film transistors (TFTs) as compiled in Table 2.[48−51] Compared with single GaSb NW device (Figure 2), the average current density of each NW gets degraded in this arrayed configuration, which is probably caused by the ineffective NW-to-NW gate coupling owing to the misalignment and fragmented wires in the device channel leading to higher parasitic capacitances. These effects would then increase the total resistance and reduce the output current. In the future, the performance of the NW arrayed device can be further enhanced through optimization of the NW print density, alignment, channel length scaling, as well as incorporation of high-k dielectrics for the top-gated configuration.

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237−4246

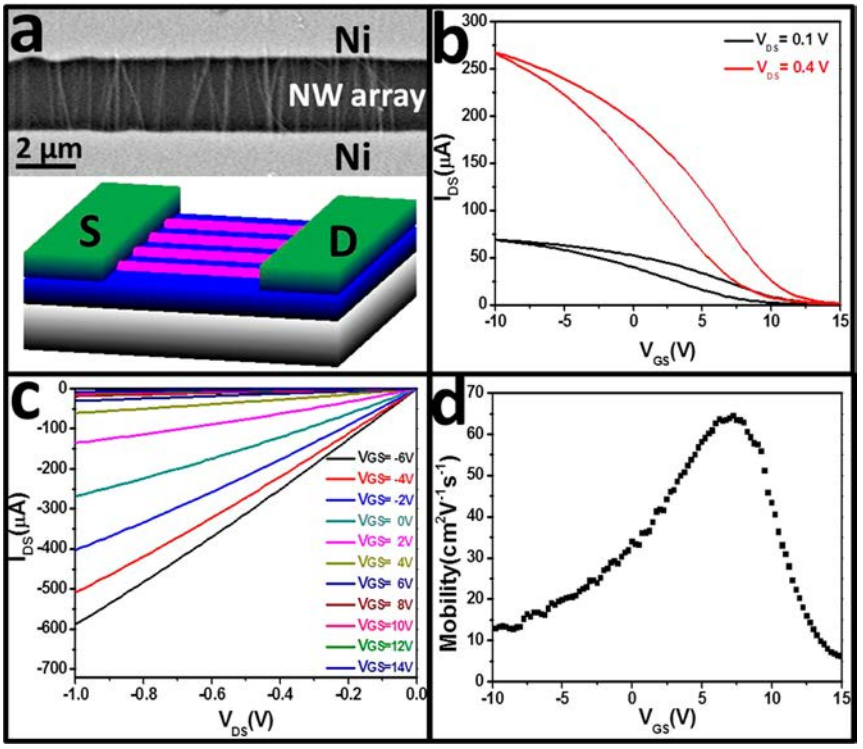


Figure 6. Electrical characterization of typical Pd-catalyzed GaSb NW parallel-arrayed FET. (a) (Top) SEM and (bottom) schematic of a back-gated Pd-GaSb NW arrayed FET. (b), (c) Transfer and output characteristics of the device. (d) Corresponding field-effect hole mobility of the device as a function of the back-gate bias.

Table 2. Hole Mobility Comparison of P-Type Thin Films

materials	hole mobility ($cm^2 V^{-1} s^{-1}$)	reference
GaSb parallel NW arrays	65	This work
Carbon nanotube parallel arrays	4.27 ± 1.62	[48]
NiOx thin film	25	[49]
Cu_2O thin film	3.9	[50]
SnO_x thin film	4.8	[51]

CONCLUSIONS

In conclusion, VSS growth of high-performance, CMOS-compatible and phase-pure ⟨111⟩-oriented GaSb NWs is successfully demonstrated with the use of Pd catalysts. Experimental results and theoretical analyses show that this particular scheme not only can narrow the diameter distribution and achieve the phase purity of grown NWs, but also maintain superior field-effect hole mobilities when fabricated into back-gated FETs, being insensitive to NW diameter variations. Compared with conventional Au-catalyzed VLS NWs, all these improvements can be attributed to the existence of immobile solid Pd_5Ga_4 catalytic seed for minimal surface diffusion and optimal in-plane orientation at the seed/NW interface during the NW nucleation. By exploiting a contact printing process, the versatility of these NWs can be further illustrated with the configuration of NW parallel-arrayed transistors. These transistors have impressive device performances, thus demonstrating that these high-performance and CMOS-compatible GaSb NWs are promising materials for a wide range of device applications.

METHODS

CMOS-Compatible GaSb NW Synthesis. CMOS-compatible metal catalysts of Pd, Ni and Cu are used for the growth of GaSb NWs by employing the surfactant-assisted solid-source CVD method as reported in our previous works.[19,20] In brief, the solid powders of GaSb (99.999% purity) and sulfur (99.99% purity) are used as the source materials. A dual-zone horizontal tube furnace, with one zone for the solid source (upstream) and another zone for the growth substrate (downstream), is used as the reactor while metal films of Pd, Ni and Cu are utilized as catalysts for the NW synthesis. Initially, catalyst films are predeposited onto Si/SiO_2 substrates (50 nm thick thermally grown), and the substrates are placed in the middle of the downstream zone. The solid sources, GaSb and sulfur powders, are next placed within two separate boron nitride crucibles, with distances of 15 and 9 cm away from the growth substrate, respectively. It is noted that the sulfur powder is actually placed in the middle of the two zones. During growth, the source and substrate are heated to the preset temperatures, accordingly. Hydrogen (99.9995% purity) is used as the carrier gas to transport the thermally vaporized materials to the downstream. Prior to heating, the pressure of the quartz tube is pumped down to 3×10^{-3} Torr and then purged with H_2 for 0.5 h. After growth, heating of the source and substrate are stopped together and the substrate is cooled down to room temperature under the hydrogen flow. At the same time, in order to confirm the VSS growth mechanism of Pd-catalyzed GaSb NWs, it is necessary to exclude any possible effect of sulfur surfactant on the NW growth mechanism; therefore, a control experiment with the GaSb NWs grown without any sulfur surfactant is also performed. The optimal growth conditions of GaSb NWs are given in Table S1.

Material Characterization. Surface morphologies of the grown NWs are examined using scanning electron microscope (SEM, FEI Company, Oregon, USA/Philips XL30, Philips Electronics, Amsterdam, Netherlands) and transmission electron microscope (TEM, Philips CM-20). Crystal structures are determined by collecting XRD pattern on a Philips powder diffractometer using Cu Kα radiation (λ = 1.5406 Å) and imaging with a high resolution TEM (HRTEM, JEOL 2100F, JEOL Co., Ltd., Tokyo, Japan). Elemental mappings are performed using an energy dispersive X-ray (EDS) detector attached to a JEOL 2100F, and the chemical composition of the obtained NWs is measured. For the TEM studies, the NWs are first suspended in ethanol solution by ultrasonication and then drop-casted onto the grid for the corresponding characterization.

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237−4246

Single Nanowire FET Fabrication and Electrical Measurements. NW FETs are fabricated by drop-casting the NW suspension onto highly doped p-type Si substrates with a 50 nm thick thermally grown gate oxide layer. Photolithography is employed to define the source/drain regions, and the 60 nm thick Ni film is thermally deposited as the contact electrodes followed by a lift-off process. The electrical performance of the fabricated back-gated FETs is then characterized with a standard electrical probe station and an Agilent 4155C semiconductor analyzer (Agilent Technologies, California, USA).

NW Parallel-Arrayed Device Fabrication and Characterization. NW parallel arrays are printed on the same type of degenerately doped p-type SiO_2/Si substrates using the well-established contact printing method.[47] These printed substrates are then spin-coated with LOR and AZ5206 photoresists, which were patterned using standard UV lithography and development, followed by Ni electrode deposition and lift-off. Electrical performance of the fabricated NW-array FETs is next characterized with a standard electrical probe station and Agilent 4155C semiconductor analyzer.

Simulation Methods. The structural optimization of the Pd_xGa_y bulk alloys is obtained by calculating their corresponding total energies. In order to simplify the calculation, a 64-atom supercell with a diamond structure is considered. The Pd and Ga atoms randomly occupy the supercell sites until the composition matches with the experimental result. Using the Vienna *ab initio* simulation package,[52,53] the geometrical structure of all the supercells is optimized to attain the most stable structure. The surface structure, consisting of a 10 layer slab and a 15 Å thick vacuum layer, is modeled. The two layers on the bottom are fixed in order to mimic the bulk, and the surface reconstructions are carried out until all forces on the free ions converging to 0.01 eV/Å. The Monkhorst−Pack *k*-point meshes of $4 \times 4 \times 1$, $4 \times 4 \times 1$, $4 \times 5 \times 1$ and $4 \times 5 \times 1$ are used for (001), (111), (110) and (211) surfaces, which have been tested for the convergence. The kinetic energy cutoff for the plane-wave basis set is 500 eV. The formula for calculating surface energies of different surfaces can be written as[54]

$$\gamma_s = (E_s - E_b)/2A$$

where E_s is the energy of the crystal with two surfaces, E_b is the energy of the bulk with the same amount of the atoms, and A is the area of the surface. The total surface free energy can be expressed in terms of the edge surface free energy of GaPd nanowires such that $E = \gamma_s S_s$, where γ_s and S_s are the surface energy and the surface area of different surfaces.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.7b01217.

Morphology of the as-prepared CMOS compatible GaSb NWs grown by 1 nm (nominal thickness) catalyst films of Ni and Cu; Structural characterization, diameter distributions and morphology of as-prepared GaSb NWs; Growth orientations of the Pd-catalyzed GaSb NWs; Transfer characteristics of a typical device fabricated with the Pd-catalyzed GaSb NW channel; Characterization of the chemical composition, morphology and crystal structure of a representative Pd-catalyzed GaSb NW; Electron microscopic characterization of the Pd-catalyzed GaSb NWs with different tip lengths; Epitaxial growth model of Pd-catalyzed GaSb NWs; Morphology of the Pd-catalyzed GaSb NWs prepared without using any surfactant in the growth process; Statistics and compilation of the Pd_5Ga_4 catalyst tips; AFM characterization of the annealed catalyst seeds; the optimal growth conditions of GaSb NWs performed in this study (PDF)

AUTHOR INFORMATION

Corresponding Authors

*E-mail: nhan@ipe.ac.cn.
*E-mail: johnnyho@cityu.edu.hk.

ORCID

Xinglong Wu: 0000-0002-2787-3069
Johnny C. Ho: 0000-0003-3000-8794

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

We acknowledge "Qilu young scholar" program of Shandong University, the General Research Fund (CityU 11204614) and the Theme-based Research Scheme (T42-103/16-N) of the Research Grants Council of Hong Kong SAR, China, the National Natural Science Foundation of China (Grants 11404162, 51672229 and 61504151), the State Key Laboratory of Multiphase Complex Systems (MPCS-2015-A-04), the Science Technology and Innovation Committee of Shenzhen Municipality (Grant JCYJ20160229165240684), the PAPD and Natural Science Foundations of Jiangsu Province (Grant BK20130549). We also acknowledge computational resources of High Performance Computing Center of Nanjing University.

REFERENCES

(1) Duan, X.; Huang, Y.; Cui, Y.; Wang, J.; Lieber, C. M. Indium Phosphide Nanowires as Building Blocks for Nanoscale Electronic and Optoelectronic Devices. *Nature* **2001**, *409*, 66−69.

(2) Gudiksen, M. S.; Lauhon, L. J.; Wang, J.; Smith, D. C.; Lieber, C. M. Growth of Nanowire Superlattice Structures for Nanoscale Photonics and Electronics. *Nature* **2002**, *415*, 617−620.

(3) Del Alamo, J. A. Nanometre-Scale Electronics with III-V Compound Semiconductors. *Nature* **2011**, *479*, 317−323.

(4) Tomioka, K.; Yoshimura, M.; Fukui, T. A III-V Nanowire Channel on Silicon for High-Performance Vertical Transistors. *Nature* **2012**, *488*, 189−192.

(5) Pribiag, V.; Nadj-Perge, S.; Frolov, S.; Van Den Berg, J.; Van Weperen, I.; Plissard, S.; Bakkers, E.; Kouwenhoven, L. Electrical Control of Single Hole Spins in Nanowire Quantum Dots. *Nat. Nanotechnol.* **2013**, *8*, 170−174.

(6) Cheung, H.-Y.; Yip, S.; Han, N.; Dong, G.; Fang, M.; Yang, Z.-x.; Wang, F.; Lin, H.; Wong, C.-Y.; Ho, J. C. Modulating Electrical Properties of InAs Nanowires *via* Molecular Monolayers. *ACS Nano* **2015**, *9*, 7545−7552.

(7) Han, N.; Yang, Z.-x.; Wang, F.; Yip, S.; Li, D.; Hung, T. F.; Chen, Y.; Ho, J. C. Crystal Orientation Controlled Photovoltaic Properties of Multilayer GaAs Nanowire Arrays. *ACS Nano* **2016**, *10*, 6283−6290.

(8) Wallentin, J.; Anttu, N.; Asoli, D.; Huffman, M.; Åberg, I.; Magnusson, M. H.; Siefer, G.; Fuss-Kailuweit, P.; Dimroth, F.; Witzigmann, B. InP Nanowire Array Solar Cells Achieving 13.8% Efficiency by Exceeding the Ray Optics Limit. *Science* **2013**, *339*, 1057−1060.

(9) Yang, Z.-x.; Han, N.; Wang, F.; Cheung, H.-Y.; Shi, X.; Yip, S.; Hung, T.; Lee, M. H.; Wong, C.-Y.; Ho, J. C. Carbon Doping of InSb Nanowires for High-Performance P-Channel Field-Effect-Transistors. *Nanoscale* **2013**, *5*, 9671−9676.

(10) Fang, H.; Hu, W.; Wang, P.; Guo, N.; Luo, W.; Zheng, D.; Gong, F.; Luo, M.; Tian, H.; Zhang, X. Visible Light-Assisted High-Performance Mid-Infrared Photodetectors Based on Single InAs Nanowire. *Nano Lett.* **2016**, *16*, 6416−6424.

(11) Miao, J.; Hu, W.; Guo, N.; Lu, Z.; Zou, X.; Liao, L.; Shi, S.; Chen, P.; Fan, Z.; Ho, J. C. Single InAs Nanowire Room-Temperature near-Infrared Photodetectors. *ACS Nano* **2014**, *8*, 3628−3635.

(12) Ma, L.; Hu, W.; Zhang, Q.; Ren, P.; Zhuang, X.; Zhou, H.; Xu, J.; Li, H.; Shan, Z.; Wang, X. Room-Temperature near-Infrared Photo-

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237−4246

detectors Based on Single Heterojunction Nanowires. *Nano Lett.* **2014**, *14*, 694−698.
(13) Xu, G.; Huang, S.; Wang, X.; Yu, B.; Zhang, H.; Yang, T.; Xu, H.; Dai, L. Synthesis, Properties, and Top-Gated Metal−Oxide−Semiconductor Field-Effect Transistors of P-Type GaSb Nanowires. *RSC Adv.* **2013**, *3*, 19834−19839.
(14) Dey, A. W.; Svensson, J.; Borg, B. M.; Ek, M.; Wernersson, L.-E. Single InAs/GaSb Nanowire Low-Power CMOS Inverter. *Nano Lett.* **2012**, *12*, 5593−5597.
(15) Ganjipour, B.; Dey, A. W.; Borg, B. M.; Ek, M.; Pistol, M.-E.; Dick, K. A.; Wernersson, L.-E.; Thelander, C. High Current Density Esaki Tunnel Diodes Based on GaSb-InAsSb Heterostructure Nanowires. *Nano Lett.* **2011**, *11*, 4222−4226.
(16) Yang, Z.-x.; Wang, F.; Han, N.; Lin, H.; Cheung, H.-Y.; Fang, M.; Yip, S.; Hung, T.; Wong, C.-Y.; Ho, J. C. Crystalline GaSb Nanowires Synthesized on Amorphous Substrates: From the Formation Mechanism to P-Channel Transistor Applications. *ACS Appl. Mater. Interfaces* **2013**, *5*, 10946−10952.
(17) Luo, T.; Liang, B.; Liu, Z.; Xie, X.; Lou, Z.; Shen, G. Single-GaSb-Nanowire-Based Room Temperature Photodetectors with Broad Spectral Response. *Sci. Bull.* **2015**, *60*, 101−108.
(18) Ganjipour, B.; Nilsson, H. A.; Mattias Borg, B.; Wernersson, L.-E.; Samuelson, L.; Xu, H.; Thelander, C. GaSb Nanowire Single-Hole Transistor. *Appl. Phys. Lett.* **2011**, *99*, 262104.
(19) Yang, Z.-x.; Han, N.; Fang, M.; Lin, H.; Cheung, H.-Y.; Yip, S.; Wang, E.-J.; Hung, T.; Wong, C.-Y.; Ho, J. C. Surfactant-Assisted Chemical Vapour Deposition of High-Performance Small-Diameter GaSb Nanowires. *Nat. Commun.* **2014**, *5*, 5249.
(20) Yang, Z.-x.; Yip, S.; Li, D.; Han, N.; Dong, G.; Liang, X.; Shu, L.; Hung, T. F.; Mo, X.; Ho, J. C. Approaching the Hole Mobility Limit of GaSb Nanowires. *ACS Nano* **2015**, *9*, 9268−9275.
(21) Love, J. C.; Wolfe, D. B.; Haasch, R.; Chabinyc, M. L.; Paul, K. E.; Whitesides, G. M.; Nuzzo, R. G. Formation and Structure of Self-Assembled Monolayers of Alkanethiolates on Palladium. *J. Am. Chem. Soc.* **2003**, *125*, 2597−2609.
(22) Allen, J. E.; Hemesath, E. R.; Perea, D. E.; Lensch-Falk, J. L.; Li, Z.; Yin, F.; Gass, M. H.; Wang, P.; Bleloch, A. L.; Palmer, R. E. High-Resolution Detection of Au Catalyst Atoms in Si Nanowires. *Nat. Nanotechnol.* **2008**, *3*, 168−173.
(23) Bar-Sadan, M.; Barthel, J.; Shtrikman, H.; Houben, L. Direct Imaging of Single Au Atoms within GaAs Nanowires. *Nano Lett.* **2012**, *12*, 2352−2356.
(24) Hannon, J.; Kodambaka, S.; Ross, F.; Tromp, R. The Influence of the Surface Migration of Gold on the Growth of Silicon Nanowires. *Nature* **2006**, *440*, 69−71.
(25) Hofmann, S.; Sharma, R.; Wirth, C. T.; Cervantes-Sodi, F.; Ducati, C.; Kasama, T.; Dunin-Borkowski, R. E.; Drucker, J.; Bennett, P.; Robertson, J. Ledge-Flow-Controlled Catalyst Interface Dynamics During Si Nanowire Growth. *Nat. Mater.* **2008**, *7*, 372−375.
(26) Pals, J. Properties of Au, Pt, Pd and Rh Levels in Silicon Measured with a Constant Capacitance Technique. *Solid-State Electron.* **1974**, *17*, 1139−1145.
(27) Sze, S. *Physics of Semiconductor Devices*; John Wiley & Sons. Inc.: New York, 1981.
(28) Schmidt, V.; Wittemann, J. V.; Senz, S.; Gösele, U. Silicon Nanowires: A Review on Aspects of Their Growth and Their Electrical Properties. *Adv. Mater.* **2009**, *21*, 2681−2702.
(29) Wolfe, D. B.; Love, J. C.; Paul, K. E.; Chabinyc, M. L.; Whitesides, G. M. Fabrication of Palladium-Based Microelectronic Devices by Microcontact Printing. *Appl. Phys. Lett.* **2002**, *80*, 2222−2224.
(30) Ford, A. C.; Ho, J. C.; Fan, Z.; Ergen, O.; Altoe, V.; Aloni, S.; Razavi, H.; Javey, A. Synthesis, Contact Printing, and Device Characterization of Ni-Catalyzed, Crystalline InAs Nanowires. *Nano Res.* **2008**, *1*, 32−39.
(31) Ford, A. C.; Ho, J. C.; Chueh, Y.-L.; Tseng, Y.-C.; Fan, Z.; Guo, J.; Bokor, J.; Javey, A. Diameter-Dependent Electron Mobility of InAs Nanowires. *Nano Lett.* **2008**, *9*, 360−365.
(32) Kranzer, D. Mobility of Holes of Zinc-Blende III-V and II-VI Compounds. *Phys. Status Solidi A* **1974**, *26*, 11−52.
(33) Wiley, J. Mobility of Holes in III-V Compounds. *Semicond. Semimetals* **1975**, *10*, 91−174.
(34) Kang, K.; Kim, D. A.; Lee, H. S.; Kim, C. J.; Yang, J. E.; Jo, M. H. Low-Temperature Deterministic Growth of Ge Nanowires Using Cu Solid Catalysts. *Adv. Mater.* **2008**, *20*, 4684−4690.
(35) Han, N.; Hui, A. T.; Wang, F.; Hou, J. J.; Xiu, F.; Hung, T.; Ho, J. C. Crystal Phase and Growth Orientation Dependence of GaAs Nanowires on Ni_xGa_y Seeds *via* Vapor-Solid-Solid Mechanism. *Appl. Phys. Lett.* **2011**, *99*, 083114.
(36) Wang, Y.; Schmidt, V.; Senz, S.; Gösele, U. Epitaxial Growth of Silicon Nanowires Using an Aluminium Catalyst. *Nat. Nanotechnol.* **2006**, *1*, 186−189.
(37) Lensch-Falk, J. L.; Hemesath, E. R.; Perea, D. E.; Lauhon, L. J. Alternative Catalysts for VSS Growth of Silicon and Germanium Nanowires. *J. Mater. Chem.* **2009**, *19*, 849−857.
(38) Xu, H.-Y.; Guo, Y.-N.; Liao, Z.-M.; Sun, W.; Gao, Q.; Hoe Tan, H.; Jagadish, C.; Zou, J. Catalyst Size Dependent Growth of Pd-Catalyzed One-Dimensional InAs Nanostructures. *Appl. Phys. Lett.* **2013**, *102*, 203108.
(39) Han, N.; Wang, F.; Hou, J. J.; Yip, S.; Lin, H.; Fang, M.; Xiu, F.; Shi, X.; Hung, T.; Ho, J. C. Manipulated Growth of GaAs Nanowires: Controllable Crystal Quality and Growth Orientations *via* a Supersaturation-Controlled Engineering Process. *Cryst. Growth Des.* **2012**, *12*, 6243−6249.
(40) Han, N.; Wang, F.; Hou, J. J.; Xiu, F.; Yip, S.; Hui, A. T.; Hung, T.; Ho, J. C. Controllable P-N Switching Behaviors of GaAsNanowires *via* an Interface Effect. *ACS Nano* **2012**, *6*, 4428−4433.
(41) Schmidt, V.; Senz, S.; Gösele, U. Diameter-Dependent Growth Direction of Epitaxial Silicon Nanowires. *Nano Lett.* **2005**, *5*, 931−935.
(42) Wang, F.; Yip, S.; Han, N.; Fok, K.; Lin, H.; Hou, J. J.; Dong, G.; Hung, T.; Chan, K.; Ho, J. C. Surface Roughness Induced Electron Mobility Degradation in InAs Nanowires. *Nanotechnology* **2013**, *24*, 375202.
(43) Hou, J. J.; Wang, F.; Han, N.; Zhu, H.; Fok, K.; Lam, W.; Yip, S.; Hung, T.; Lee, J. E.-Y.; Ho, J. C. Diameter Dependence of Electron Mobility in InGaAs Nanowires. *Appl. Phys. Lett.* **2013**, *102*, 093112.
(44) Okamoto, H. Ga-Pd (Gallium-Palladium). *J. Phase Equilib. Diffus.* **2008**, *29*, 466−467.
(45) Algra, R. E.; Vonk, V.; Wermeille, D.; Szweryn, W. J.; Verheijen, M. A.; van Enckevort, W. J.; Bode, A. A.; Noorduin, W. L.; Tancini, E.; de Jong, A. E. Formation of Wurtzite InP Nanowires Explained by Liquid-Ordering. *Nano Lett.* **2010**, *11*, 44−48.
(46) Elliott, R. P.; Shunk, F. A. The Au-Ga (Gold-Gallium) System. *Bull. Alloy Phase Diagrams* **1981**, *2*, 356−358.
(47) Fan, Z.; Ho, J. C.; Jacobson, Z. A.; Yerushalmi, R.; Alley, R. L.; Razavi, H.; Javey, A. Wafer-Scale Assembly of Highly Ordered Semiconductor Nanowire Arrays by Contact Printing. *Nano Lett.* **2008**, *8*, 20−25.
(48) Chen, K.; Gao, W.; Emaminejad, S.; Kiriya, D.; Ota, H.; Nyein, H. Y. Y.; Takei, K.; Javey, A. Printed Carbon Nanotube Electronics and Sensor Systems. *Adv. Mater.* **2016**, *28*, 4397−4414.
(49) Shan, F.; Liu, A.; Zhu, H.; Kong, W.; Liu, J.; Shin, B.; Fortunato, E.; Martins, R.; Liu, G. High-Mobility P-Type Niox Thin-Film Transistors Processed at Low Temperatures with Al_2O_3 High-K Dielectric. *J. Mater. Chem. C* **2016**, *4*, 9438−9444.
(50) Fortunato, E.; Figueiredo, V.; Barquinha, P.; Elamurugu, E.; Barros, R.; Gonçalves, G.; Park, S.-H. K.; Hwang, C.-S.; Martins, R. Thin-Film Transistors Based on P-Type Cu_2O Thin Films Produced at Room Temperature. *Appl. Phys. Lett.* **2010**, *96*, 192102.
(51) Fortunato, E.; Barros, R.; Barquinha, P.; Figueiredo, V.; Park, S.-H. K.; Hwang, C.-S.; Martins, R. Transparent P-Type SnO_X Thin Film Transistors Produced by Reactive Rf Magnetron Sputtering Followed by Low Temperature Annealing. *Appl. Phys. Lett.* **2010**, *97*, 052105.
(52) Blöchl, P. E. Projector Augmented-Wave Method. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1994**, *50*, 17953.
(53) Kresse, G.; Joubert, D. From Ultrasoft Pseudopotentials to the Projector Augmented-Wave Method. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1999**, *59*, 1758.

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237−4246

(54) Liu, L.; Wu, X.; Li, T.; Chu, P. K. Twinning $Ge_{0.54}Si_{0.46}$ Nanocrystal Growth Mechanism in Amorphous SiO_2 Films. *Appl. Phys. Lett.* **2010**, *96*, 173111.

DOI: 10.1021/acsnano.7b01217
ACS Nano 2017, 11, 4237−4246