ZnO Nanofiber Thin-Film Transistors with Low-Operating Voltages

Fengyun Wang, Longfei Song, Hongchao Zhang, You Meng, Linqu Luo, Yan Xi, Lei Liu, Ning Han, Zaixing Yang, Jie Tang, Fukai Shan,* and Johnny C. Ho*

Although significant progress has been made towards using ZnO nanofibers (NFs) in future high-performance and low-cost electronics, they still suffer from insufficient device performance caused by substantial surface roughness (i.e., irregularity) and granular structure of the obtained NFs. Here, a simple one-step electrospinning process (i.e., without hot-press) is presented to obtain controllable ZnO NF networks to achieve high-performance, large-scale, and low-operating-power thin-film transistors. By precisely manipulating annealing temperature during NF fabrication, their crystallinity, grain size distribution, surface morphology, and corresponding device performance can be regulated reliably for enhanced transistor performances. For the optimal annealing temperature of 500 °C, the device exhibits impressive electrical characteristics, including a small positive threshold voltage ($V_{th}$) of $\approx 0.9$ V, a low leakage current of $\approx 10^{-12}$ A, and a superior on/off current ratio of $\approx 10^6$, corresponding to one of the best-performed ZnO NF devices reported to date. When high-$\kappa$ AlO$_x$ thin films are employed as gate dielectrics, the source/drain voltage ($V_{DS}$) can be substantially reduced by 10x to a range of only 0–3 V, along with a 10x improvement in mobility to a respectable value of $0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. These results indicate the potential of these nanofibers for use in next-generation low-power devices.

1. Introduction

In the past decade, thin-film transistors (TFTs) based on the unique 1D semiconductors as active device layers have been extensively investigated and explored for various technological applications in photodetectors, chemical and biological sensors, active matrix organic light emitting diodes, and so on. Among these 1D nanomaterials, many novel synthesis techniques have then been developed, including chemical vapor deposition (CVD), hydrothermal methods, and template-assisted electrodeposition, etc; however, all of these fabrication schemes come with different process-related disadvantages. For example, CVD has been widely employed for the growth of 1D semiconductor nanostructures, in which this technique is still far from being compatible with the large-scale manufacturing platform due to the rather high fabricating cost, rigorous process control, low production throughput, and complicated subsequent device fabrication scheme. Although hydrothermal methods are seem to be the simple process and capable to produce large amounts of 1D nanomaterials with the relatively low cost, they are challenging to precisely control the diameter, morphology, and crystal structure of the nanomaterials obtained, seriously limiting their practical utilizations. In general, electrospinning is well accepted to its simplicity and versatility to yield organic, inorganic or composite nanofibers (NFs). This technique can not only fabricate NFs with well-controlled properties, such as the excellent crystallinity, homogeneous chemical composition, and uniform diameters but also deliver the high throughput their chemical and physical properties, eventually limiting their practical utilizations. In general, electrospinning is well accepted to its simplicity and versatility to yield organic, inorganic or composite nanofibers (NFs). This technique can not only fabricate NFs with well-controlled properties, such as the excellent crystallinity, homogeneous chemical composition, and uniform diameters but also deliver the high throughput

DOI: 10.1002/aelm.201700336
production of NFs, which illustrates promising perspectives of deploying electrospun NFs for next-generation high-performance electronic devices.

At the same time, owing to the superior electrical properties, chemical stability, and environmental friendliness, metal-oxide nanomaterials are usually considered as the ideal channel materials for TFTs.[23,24] In particular, In2O3 and ZnO have been the illustrating examples of high-performance metal-oxide nanomaterials as they consist of the relatively high electron mobility as well as the large bandgap for excellent transmittance in the visible region.[25] Nonetheless, the In-based metal oxides are not the ideal semiconductor materials for large-area integrated circuits because of the scarcity of In.[26–28] As a result, ZnO is not the ideal semiconductor material for large-area integrated electronic devices.[29–31] In this regard, the metal-oxide semiconductors typically require a thermal annealing process. In specific, the NFs are first investigated with different annealing temperatures, ranging from 450 to 600°C. Uniform network is further increased to 600°C, the NF would start to significantly overflow to give discrete and disconnected NF segments as marked in the region of yellow boxed in Figure 1c. Moreover, the zoom-in SEM is employed to evaluate the diameter and to verify the surface morphology of NFs annealed at different temperatures (Figure 1 and Figure S1 (Supporting Information), the as-spun ZnO NFs are randomly aligned on the receiver substrate as NF networks because of the bending instability of the whipping process. In specific, the NFs are first investigated with different annealing temperatures, ranging from 450 to 600°C. Uniform and continuous ZnO NFs are obtained for the annealing temperature of between 450 and 550°C. In this temperature range, when the temperature is increased, the NF surface becomes rougher, which would in principle act as the surface scattering site to disturb the carrier transport along the NF, reducing the carrier mean free time and mobility.[43,44] When the temperature is further increased to 600°C, the NF would start to significantly overflow to give discrete and disconnected NF segments as marked in the region of yellow boxed in Figure 1c. Moreover, the zoom-in SEM is employed to evaluate the diameter and to verify the surface morphology of NFs annealed at different temperatures (Figure 1 and Figure S1, Supporting Information). Based on the statistics of more than 50 individual NFs for each sample group, the average diameters of NFs are observed to be 66.5 ± 4.2, 60.5 ± 5.0, 55.5 ± 3.5, and 58.5 ± 3.0 nm for the annealing temperatures of 450, 500, 550, and 600°C, respectively (Figure 1f). This statistic demonstrates clearly that the diameter of ZnO NFs decreases as the annealing temperature increases, which is consistent to the results obtained from thermogravimetric analysis (TGA) curve presented in Figure S2 (Supporting Information), examining thermal properties of the starting ZnO precursor solutions. These trends of the diameter reduction and the surface roughness upturn for the increasing annealing temperature can be attributed to the degradation of organic residues decomposed from polyvinylpyrrolidone (PVP) salt is selected as the zinc precursor due to its relatively low decomposition temperature and high solubility, which is crucial to achieve superior electrical properties of the electrospun NFs. Since the nonuniform size distribution of nanograins existed within the ZnO NFs is found to yield poor electrical properties, such as the high off current, low saturation current, and reduced carrier mobility,[40,41] we systematically assess the effect of different annealing temperatures on the surface morphology, crystallinity, and electrical properties of the electrospun ZnO NFs. When the annealing is optimized at 500°C, the fabricated NF device exhibits the respectable electrical performance with a low leakage current of ≈10−12 A, which could have the superior pixel retention in display applications, a relatively high on/off current ratio of ≈106, being highly preferred in electronic switching devices, and a small positive threshold voltage (Vth) of ≈0.9 V, that is attractive for the energy-efficient devices. With the aim to further decrease their operation voltages, solution-processed ALD thin film is also employed as the high-k dielectric layer for the device construction and the corresponding operation voltage (e.g., source/drain voltage) can then be significantly reduced from 30 to 3 V. All these results indicate evidently the technological potency of our ZnO NF TFTs for the future high-performance, low-cost, large-area, and low-operating power electronics.

2. Results and Discussions

As shown in the scanning electron microscope (SEM) images in Figure 1 and Figure S1 (Supporting Information), the as-spun ZnO NFs are randomly aligned on the receiver substrate as NF networks because of the bending instability of the whipping process. In specific, the NFs are first investigated with different annealing temperatures, ranging from 450 to 600°C. Uniform and continuous ZnO NFs are obtained for the annealing temperature of between 450 and 550°C. In this temperature range, when the temperature is increased, the NF surface becomes rougher, which would in principle act as the surface scattering site to disturb the carrier transport along the NF, reducing the carrier mean free time and mobility.[43,44] When the temperature is further increased to 600°C, the NF would start to significantly overflow to give discrete and disconnected NF segments as marked in the region of yellow boxed in Figure 1c. Moreover, the zoom-in SEM is employed to evaluate the diameter and to verify the surface morphology of NFs annealed at different temperatures (Figure 1 and Figure S1, Supporting Information). Based on the statistics of more than 50 individual NFs for each sample group, the average diameters of NFs are observed to be 66.5 ± 4.2, 60.5 ± 5.0, 55.5 ± 3.5, and 58.5 ± 3.0 nm for the annealing temperatures of 450, 500, 550, and 600°C, respectively (Figure 1f). This statistic demonstrates clearly that the diameter of ZnO NFs decreases as the annealing temperature increases, which is consistent to the results obtained from thermogravimetric analysis (TGA) curve presented in Figure S2 (Supporting Information), examining thermal properties of the starting ZnO precursor solutions. These trends of the diameter reduction and the surface roughness upturn for the increasing annealing temperature can be attributed to the degradation of organic residues decomposed from polyvinylpyrrolidone (PVP)
and the enhanced diffusion rate of Zn atoms. Notably, there is a slight increase of the NF diameter at the temperature of 600 °C as compared with the one of 550 °C, which is probably caused by the dominating role of the nanocrystal growth along the NF. The reduction of nanofiber diameters from 450 to 550 °C is mostly due to the PVP degradation, while, for the nanofibers annealed at 600 °C, the increase of diameters is dominated by the grain growth. Based on the TGA analysis, the PVP precursor could not be completely decomposed at 450 °C or the lower temperature. This way, the residual carbon compounds would disorganize the Zn–O–Zn lattice, potentially acting as the electron transport channel even though the NFs have the smooth surface.[45] When the annealing temperature is increased to 600 °C, the organics within the NFs can be completely decomposed, whereas the ZnO nanoparticles would grow into large crystallites and eventually result into the discrete NF segments for the degraded electrical properties. It is obvious that the appropriate process window of the annealing temperature is narrow at ≈500 °C for the uniform diameter and continuous surface morphology. Besides, the diameter of nanofibers can also be precisely controlled by the distance between the needle tip and the collector, orifice size of the needle, and the electric potential applied between the needle tip and the collector. The density of the nanofibers can as well be regulated by controlling electrospinning time.

Next, X-ray diffusion (XRD) is performed to evaluate the crystallinity of ZnO NFs annealed with different temperatures as depicted in Figure 2. It is noted that when the NFs are annealed at 400 °C and higher, the XRD spectra exhibit nine distinct peaks at 31.75°, 34.41°, 36.23°, 47.51°, 56.57°, 62.84°, 66.36°, 67.93°, and 69.07°, corresponding to (100), (002), (101), (102), (110), (200), (112), and (201) lattice planes of ZnO (JCPDS, No. 80-0075), accordingly, which confirms the existence of crystalline ZnO NFs. There are not any impurities and secondary phases observed in the spectra, demonstrating the high purity of the products. With the increase of the annealing temperature, the diffraction peaks of ZnO NFs become sharper and more intense, which indicate the improvement of the crystallinity and the grain size of NFs obtained. Importantly, the grain size of ZnO nanoparticles existed in the NFs annealed at different temperatures can be assessed from XRD spectra by the Scherrer equation

$$D = \frac{K\lambda}{\beta\cos\theta}$$

where \(K\) is Scherrer constant, \(\lambda\) is the wavelength of X-rays, \(\beta\) is the full width of half-maximum of the diffraction peak, and
\( \theta \) is the diffraction angle. This way, the grain size of ZnO nanoparticles can be determined as \( \approx 15.3, \approx 20.7, \approx 24.7, \) and \( \approx 32.4 \) nm with the annealing temperature of 450, 500, 550, and 600 \( ^\circ \text{C} \), respectively. All these clearly illustrate the grain size getting larger with the increasing annealing temperature, which can be simply explained by the following Equation (2) correlating the relationship between growth speed of crystal grain and growth temperature

\[
v = k \exp \left( \frac{-\Delta G^*}{RT} \right)
\]

where \( v \) is the growth speed of crystal grain, \( k \) and \( R \) are both constants, and \( \Delta G^* \) is the growth activation energy which is an inherent material property. As \( \Delta G^* \) is fixed, the growth speed \( v \) follows the Arrhenius relationship of the growth temperature. Explicitly, the grain size would grow persistently with the increasing annealing temperature. As discussed above, when the gains grow too large, the NFs would have rough surface and become discrete NF segments giving rise to inferior electrical properties; hence, the high annealing temperature should be avoided. Similar phenomena has also been observed in other nanomaterial system, such as In\(_2\)O\(_3\), even though the grain size existed in the electrospun ZnO NFs is larger than that of In\(_2\)O\(_3\) NFs due to its enhanced diffusion of ZnO constituents at the same annealing temperature. \[46\]

Apart from the crystallinity, it is also important to further understand the microstructure evolution of ZnO NFs annealed at various temperatures. As displayed in the high-resolution transmission electron microscope (HRTEM) images in Figure 3 and Figure S3 (Supporting Information), when the annealing temperature is 500 \( ^\circ \text{C} \), the NF is highly uniform in its diameter and is composed of nanograins exhibiting polycrystalline structure. The fast Fourier transform (FFT) image (Figure 3b inset) can confirm again the polycrystalline nature with the diffraction rings. Based on the HRTEM images, the average NF grain size can be determined as \( \approx 11.5, \approx 14.6, \approx 17.5, \) and \( \approx 26.1 \) nm for the annealing temperature of 450, 500, 550, and 600 \( ^\circ \text{C} \), respectively, in which the trend is perfectly consistent to the one calculated from XRD spectrum (Figure 3d). Furthermore, the interplanar spacings of (101) and (100) are measured to be \( \approx 0.252 \) and \( \approx 0.284 \) nm, respectively, in Figure 3c, in which they are very close to the ideal interplanar spacing of cubic ZnO material (e.g., 0.248 nm for the (101) planes) as compared with the ones annealed at other temperatures, indicating the formation of stoichiometric and high-quality ZnO NFs annealed at 500 \( ^\circ \text{C} \). It is also worth noting that the NFs annealed at \( \approx 600 \) \( ^\circ \text{C} \) are broken into individual ZnO nanoparticles (Figure S3f, Supporting Information) during the preparation of TEM sample by ultrasonication, which further demonstrates the fragility of ZnO NFs processed at such high temperature.

In the meanwhile, X-ray photoelectron spectroscopy (XPS) is as well performed to better understand the local bonding differences among ZnO NFs fabricated with various annealing temperatures. As demonstrated in the typical XPS spectra of different ZnO NFs in Figure 4, the O 1s spectra can be deconvoluted into two principal signatures, namely the O (1) peak representing the M–O–M bonding located at 529.8 \( \pm \) 0.1 eV, where M is the metal species, as well as the O (2) peak designating the surface metal hydroxide (M–OH) bonding and the weakly bound species (M–OR), such as CO\(_2\) and H\(_2\)O located at 531.2 \( \pm \) 0.1 eV. \[47\] As the annealing temperature increases from 400 to 500 \( ^\circ \text{C} \), the intensity of O (1) peaks are obviously increased as compared with the ones of O (2) peaks. When the temperature is continued to increase to 600 \( ^\circ \text{C} \), the corresponding intensity of O (1) peak is decreased slightly, which can be attributed to the fracture of NFs and reduction of the M–O–M lattice species. As the carrier transport is taken place in metal oxides highly dependent on the characteristics of M–O–M lattice, the quantity of M–O–M lattice (\( \eta_{M-O-M} \)) is a key parameter to describe their electronic transport properties. Specifically, \( \eta_{M-O-M} \) is defined as the sub-peak ratio of the M–O–M peak area to the total area of O1s peak following the Equation (3) below.\[44\]

\[
\eta_{M-O-M} = \frac{S_{M-O-M}}{S_{total}}
\]
where $S_{M-O-M}$ is the area of the M–O–M peak and $S_{total}$ is the total area of the O1s peak. The table in Figure 4 compiles the variation of $\eta_{M-O-M}$ values as the annealing temperature changes. For the annealing temperature at 500 °C, the $\eta_{M-O-M}$ value hits the highest point of 0.70, which can be deduced that the fabricated NFTFTs would exhibit the best electronic device performance (will be discussed in details in the next session). When the temperature further increases to 600 °C, the $\eta_{M-O-M}$ value decreases to some extent from 0.70 to 0.68, attributable to the fragmentation of the NFs. Overall, the $\eta_{M-O-M}$ values are extremely sensitive to the annealing temperature of ZnO NFs. Once the optimum annealing temperature of 500 °C is reached, the NFs are more favorable to form more M–O–M lattice species for the enhanced carrier transport.

In an effort to shed light on the influence of annealing temperatures on the electrical properties of NFs, numerous TFTs based on ZnO NF networks processed with different annealing temperatures are fabricated and characterized. Figure 5a demonstrates the SEM image of a representative ZnO NFTFT together with its schematic illustration configured in the global back-gated geometry. It should be noted that all devices are fabricated with the same process condition,
the identical device geometry (i.e., channel width and length of 1000 and 100 μm, respectively) and the similar NF network density, except for the annealing temperature. As we reported previously, too low or too high NF network density would influence their electrical properties.[46] In this work, the density of ZnO NF networks is controlled to ≈0.45 NF μm−2 with the electrospinning time of 30 s for all devices, in which this density is shown to exhibit the best electrical characteristics among all studied devices. Also, the same VGS sweep rate is applied to ensure a consistent comparison among all devices characterized. Figure 5b demonstrates the corresponding transfer curves ( IDV versus VGS) of ZnO NFTFTs using 300 nm thick SiO2 as the dielectric layer, ZnO NF networks annealed from 400 to 600 °C as the active channel layer and the VDS of 30 V. At the temperature of 400 °C, the NF device barely exhibits semiconductor properties. It could be deduced from TGA curves (Figure S2, Supporting Information) that there might be some amount of organic residuals existed in the NFs processed with low annealing temperatures, hindering the carrier transport. When the annealing temperature is increased from 450 to 600 °C, all the devices yield the intrinsic n-type conductivity, which could be mainly originated from the donor-like crystal defects, such as the O vacancies and/or Zn interstitials. As summarized in Table S1 (Supporting Information), the NF device performance is heavily dependent on the annealing temperature. It is worth noting that all the devices annealed at various temperatures have relatively low off current, ranging from 10−11 to 10−10 A, which is advantageous for high-speed switching devices, high-performance UV detectors, and so on, while the saturation on current changes obviously with various temperatures. For example, the ZnO NF device processed at 500 °C has an on current of ≈1.3 × 10−6 A, nearly twenty times of the magnitude larger than the devices fabricated at 450 °C, which might be caused by the complete decomposition of PVP or its residual carbon compounds. Meanwhile, the on current decreases significantly after being annealed at 550 °C as compared with that annealed at 500 °C, attributable to the surface roughness resulting in a fluctuating shape along the radial direction and leading to surface scattering sites deteriorating the electron transport along the axial direction.[48] Also, the corresponding ηM−O−M value would become smaller when the NF is annealed at 550 °C as compared with the one of 500 °C, therefore, the quantity of carrier propagation channels of ZnO NFs annealed at 550 °C is less than the ones annealed at 500 °C. In this case, when the annealing temperature is optimized at 500 °C, the NF device exhibits a considerable large on/off current ratio of ≈106, a relatively high electron mobility of ≈0.02 cm2 V−1 s−1 and a comfortably small positive Vth of ≈0.9 V. Such a small positive Vth infers that the device can operate in enhancement mode yielding a zero current at the zero gate bias, indicating the reduced power consumption during practical utilizations. It is also noted that when the fibers are annealed at 450 °C, there is still a lot of organic residue left in the channel, deteriorating the corresponding gate coupling efficiency such that the on current is extremely low. Once the annealing temperature increases from 450 to 600 °C, the location of Ioff exhibits a positive shift with the increasing annealing temperature. In specific, the Ioff is located in negative VGS at the annealing temperature of 450 °C while the corresponding Vth is extracted as 2.0 V from the IDVS2/3 versus VGS curves. This phenomenon can be attributed to the small SS value (0.31 V dec−1). Moreover, the SS is generally related with defect states and their density. When the fibers are annealed at 450 and 500 °C, their enhanced smooth surface is anticipated to reduce the surface traps and the defect density, which results in the smaller SS values and increases the VO values, transforming the device operation from depletion mode to enhancement mode. Therefore, the Ioff locations are first existed at negative VGS and changed according to the SS and Vio values. Conversely, when the fibers are annealed at 550 and 600 °C, the surface of nanofibers become rougher and even cracked, which would significantly hinder the gate coupling and transportation of carriers. This way, the corresponding Vth values and Ioff location are eventually shifted to the large positive VGS, accordingly. Here, the mobility is measured and extracted by Equation (4) in the Experimental Section and Vth is obtained in the saturation region through the maximum curvature of the IDVS2/3 versus VGS plot. In order to fully identify the variation between annealing temperatures and device performance, 10 devices are compared and contrasted for the on/off current ratio, VDS saturation on current and off current, corresponding to Figure 5d,e, and Figure S4 (Supporting Information), respectively. It is clear that the ZnO NFTFTs processed at 500 °C exhibit the best electrical performance. As depicted in the output characteristics ( IDVS versus VDS curves) of the optimized ZnO NFTFT in Figure 5f, it gives a typical n-type conducting and current saturation behaviors. In addition, at a small VO bias, the output current increases linearly with the VDS bias, indicating the electrical contact between ZnO NF networks and Al electrodes is Ohmic-like here. More importantly, when our optimized ZnO NF devices are compared against recent state-of-the-art counterparts reported in the literature (Table 1), our devices can deliver the highest electron mobility

Table 1. A comparison of electrical properties of the electrospun ZnO NFTFTs.

<table>
<thead>
<tr>
<th>Materials</th>
<th>Polarity</th>
<th>Source/drain</th>
<th>Substrate</th>
<th>μ or μI [cm2 V−1 s−1]</th>
<th>Saturation current [A]</th>
<th>Ioff/loff</th>
<th>Year</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZnO</td>
<td>n</td>
<td>copper wire/copper wire</td>
<td>SiO2/Si</td>
<td>–</td>
<td>6 × 10−11</td>
<td>104</td>
<td>2008</td>
<td>[33]</td>
</tr>
<tr>
<td>ZnO</td>
<td>n</td>
<td>Au/Au</td>
<td>SiO2/Si</td>
<td>4.6 × 10−9</td>
<td>10−9</td>
<td>&lt;10−4</td>
<td>2013</td>
<td>[34]</td>
</tr>
<tr>
<td>Ce-doped ZnO</td>
<td>P</td>
<td>An/Au</td>
<td>SiO2/Si</td>
<td>–</td>
<td>10−8</td>
<td>104</td>
<td>2014</td>
<td>[32]</td>
</tr>
<tr>
<td>La-doped ZnO</td>
<td>P</td>
<td>An/Au</td>
<td>SiO2/Si</td>
<td>–</td>
<td>10−8</td>
<td>&lt;10−4</td>
<td>2015</td>
<td>[35]</td>
</tr>
<tr>
<td>Al-doped ZnO</td>
<td>n</td>
<td>AI/Al</td>
<td>SiO2/Si</td>
<td>33 × 10−8</td>
<td>10−8</td>
<td>104</td>
<td>2016</td>
<td>[36]</td>
</tr>
<tr>
<td>ZnO</td>
<td>n</td>
<td>Ti−Au/Ti−Au</td>
<td>SiO2/Si</td>
<td>0.018</td>
<td>=nA</td>
<td>&lt;10−4</td>
<td>2016</td>
<td>[37]</td>
</tr>
<tr>
<td>Our work</td>
<td>n</td>
<td>AI/Al</td>
<td>SiO2/Si</td>
<td>0.02</td>
<td>1.26 × 10−4</td>
<td>102</td>
<td>2017</td>
<td>–</td>
</tr>
</tbody>
</table>
of \(\approx 0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}\), the largest saturation on current of \(10^{-6} \text{ A}\) and maximum on/off current ratio of \(10^6\), representing one of the best ZnO NF devices investigated so far.

In order to further reduce the operation voltage (e.g., \(V_{DS}\) of 30 V) employed above and improve the device performance, solution processed AlO\(_x\) film is used as gate dielectric layer for the device construction. As compared with other solution-processed high-k dielectrics, AlO\(_x\) is adopted here due to its relatively large-area uniformity, high dielectric constant of 6.7, excellent surface smoothness with a roughness of below 0.2 nm and almost pinhole free characteristics (e.g., low leakage current density down to 1 nA cm\(^{-1}\) at 2 MV cm\(^{-1}\) and high breakdown electric field of greater than 5 MV cm\(^{-1}\)).\(^{46}\) Importantly, this smooth surface can minimize the carrier scattering, being highly beneficial for the carrier mobility enhancement and improved device stability. Figure 6a gives the output curves of the optimized ZnO NF TFT using AlO\(_x\) dielectrics with the gate voltage (\(V_{GS}\)) stepping from 0 to 2 V in five steps, while Figure 6b illustrates the corresponding transfer curves with the \(V_{DS}\) sweeping from \(-1\) to 3 V at a fixed scan rate and a \(V_{DS}\) = 3 V. All these indicate the minimized operating voltage achieved with the use of high-\(k\) dielectrics of AlO\(_x\). The \(V_{DS}\) of 3 V here is reduced by 10 times, exhibiting the same or even better device performances, as compared with the device based on SiO\(_2\) dielectrics. Specifically, the device yields a \(V_{th}\) of \(\approx 0.42 \text{ V}\), a field-effect mobility of \(\approx 0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}\), a saturation on current of \(\approx 1.12 \times 10^{-6} \text{ A}\), an off current of \(\approx 4.32 \times 10^{-13} \text{ A}\) and an \(I_{on}/I_{off}\) of \(\approx 2.56 \times 10^6\). This significant performance enhancement can be due to the better interface quality between ZnO NF and AlO\(_x\) dielectric with the reduced interface defects and minimized interface carrier scattering. Importantly, after sweeping the gate voltage for 50 cycles, the transfer characteristics do not change significantly even without any device passivation applied to the current device configuration. The slight \(V_{th}\) shift of 0.25 V can be probably related to the interaction between unpassivated NF and ambient environment. In the future, more detailed device stability measurement, including prolonged periods of electrical stress with operating gate biases, will be performed to assess the \(V_{th}\) shift and corresponding degradation mechanism. In any case, as shown in Figure 6d and Figure S5 (Supporting Information), the on/off current ratio, the saturation on current and the off current are all relatively stable after 50 cycles of the gate voltage sweeping. These negligible changes of all device parameters suggest strongly that the optimally annealed ZnO NFs are highly crystalline with minimized surface scattering for the enhanced electronic device performance and electrical stability, being the ideal active materials for the next-generation, large-scale, and low-operating power electronic devices.

3. Conclusions

In conclusion, high-performance and low-operating power field-effect transistors based on ZnO NF networks are demonstrated with the simple one-step electrospinning method. It is found that the crystallinity, the surface morphology, and the electrical properties of NF can be simply and reliably controlled by the annealing temperature during the fiber spinning. As compared with other state-of-the-art ZnO NF devices, our optimized device exhibits one of the best NF device performance up to now, including a high saturation on current of \(\approx 1.26 \times 10^{-6} \text{ A}\), a low off current of \(\approx 1.54 \times 10^{-12} \text{ A}\), and a respectable field-effect electron mobility of \(\approx 0.04 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}\).
a small positive $V_{th}$ of $\approx 0.9$ V as well as a high $I_{on}/I_{off}$ of $\approx 10^6$. In order to further decrease the operation voltage and enhance the device characteristics, high-$\kappa$ dielectric of solution-processed AlO$_x$ thin films, instead of the conventional SiO$_2$ dielectrics, are employed for the device construction, in which the source/drain voltage can be substantially reduced by 10 times to a range of only 0 to 3 V. Also, the electron mobility can be improved by 10 times to the value of 0.2 cm$^2$ V$^{-1}$ s$^{-1}$. Importantly, all device parameters do not change significantly after 50 cycles of gate voltage sweeping, indicating the electrical stability contributed by the enhanced ZnO nanofiber device channel. All these findings reveal explicitly that the optimally annealed electrospun ZnO NFs consist of the promising potential for the high-performance, large-scale, and low-operating power electronics, such as photodetectors, gas sensor arrays, and display applications.

4. Experimental Section

Preparation of the Electrospinning Precursor: The ZnO electrospinning precursor solution was prepared by dissolving of 0.3 g zinc acetate dihydrate (Zn(C$_2$H$_5$O$_2$)$_2$$\cdot$2H$_2$O, Aladdin, 99.99%) and 0.8 g PVP (Aladdin, K88-96) into 5 g N,N-dimethylformamide (DMF, Aladdin, AR, 99.5%). Then, the above precursor solution was stirred for 5 h at room temperature ($\approx 25$ °C).

Solution Processed AlO$_x$ Thin Film Fabrication: The AlO$_x$ precursor solution was prepared by dissolving of 0.1 m aluminum nitrate nonahydrate (Al(NO$_3$)$_3$$\cdot$9H$_2$O, 99.99%, Aladdin) in 9.4 g DMF (Aladdin, AR, 99.5%) which worked as solvent. The above solution was then stirred for 5 h at room temperature ($\approx 30$–50% RH) to form crystalline ZnO NFs, conducted at the room temperature with a relative humidity of 30–50%.

In order to remove residual organics and to form crystalline ZnO NFs, the above precursor solution was stirred for 5 h at room temperature with a relative humidity of 30–50% RH. Then, the above precursor solution was stirred for 5 h at room temperature ($\approx 25$ °C).

Solution Processed AlO$_x$ Thin Film Fabrication: The AlO$_x$ precursor solution was prepared by dissolving of 0.1 m aluminum nitrate nonahydrate (Al(NO$_3$)$_3$$\cdot$9H$_2$O, 99.99%, Aladdin) in 9.4 g DMF (Aladdin, AR, 99.5%) which worked as solvent. The above solution was then stirred for 5 h at room temperature ($\approx 30$–50% RH) to form crystalline ZnO NFs, conducted at the room temperature with a relative humidity of 30–50% RH.