COMMUNICATION

Dielectric Engineering of a Boron Nitride/Hafnium Oxide Heterostructure for High-Performance 2D Field Effect Transistors

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In the past decade, based on the extensive research in graphene communities, it was realized that the dielectric environment of two-dimensional (2D) semiconductor nanostructures would play a crucial role in the carrier transport of their fabricated devices. Till now, the performance of SiO_2-supported devices has been still greatly restricted by the carrier scattering due to the oxide trapped charges,[1–3] surface roughness,[4–6] and surface optical phonons.[3,7] In order to minimize this degradation, the SiO_2 substrate can be completed removed or replaced by others. One approach is to fabricate devices by suspending the 2D channel material,[8,9] which has been realized in several graphene device structures with the significant improvement in their corresponding carrier mobilities. However, this delicate process of suspending channel materials would substantially complicate the device fabrication as well as impose limitations on the device architecture. Another tactic is to explore the alternatives to SiO_2 and it typically involves high-κ dielectrics, in which Coulombic impurity scattering is confirmed to be strongly shielded by the dielectric screening.[10] Unfortunately, it is found that charge traps and surface optical phonon scattering arising from the dielectrics would wash out this advantage.[11–13]

Recently, it has been shown that placing 2D semiconductors on hexagonal boron nitride (h-BN) can yield a drastic improvement in their corresponding carrier mobilities.[14,15] As a layered material with the honeycomb lattice crystal structure, the layered h-BN has advantages of atomically smooth surface and large surface optical phonon energy, where all these are expected to minimize the unfavorable effect of trapped charges and optical phonon scattering, respectively. Nevertheless, high mobility is not the only keypoint for high performance transistors, which should include large saturated current, small subthreshold swing, and so on. For example, the device miniaturization, including the 2D materials based complementary metal-oxide-semiconductor technology, would inevitably continue with the channel scaling beyond 10 nm or less,[16] but the relatively low dielectric constant (3–4 for bulk BN) and uncontrollable thickness of h-BN severely limit this scaling. Although the issue of dielectric environment has presented a major hurdle to achieve practical utilizations of 2D materials, there are few systematic studies performed and it remains an unresolved challenge to this moment. In this regard, the present work demonstrates a rational design of an ideal dielectric heterostructure for 2D devices, which combines the advantages of high-κ dielectric HfO_2 and few-layer h-BN. In a distinct contrast to others reporting the reduction of carrier mobility,[17] this heterostructured dielectric stack facilitates the superior field-effect mobility to be obtained in the top-gated 2D (i.e., MoS_2 and graphene) device operation not only by suppressing the charge traps and surface optical phonon scattering at the channel/dielectric interface but also maintaining the enhancement of effective gate capacitance. Furthermore, this dielectric heterostructure can also be applied and extended to other conventional 2D device systems such as GaN-thin-film-based high-electron-mobility transistors (HEMTs), which indicate its versatility for the advanced electronic devices.

In this design of dielectric heterostructure, there are two major criteria for the consideration: (i) the first dielectric layer directly put down above the channel for the minimization of channel surface roughness, charge traps and optical phonon scattering; (ii) the second dielectric layer for the alleviation of

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Coulombic scattering and enhancement of the effective gate capacitance. In order to achieve these two requirements, the few-layer h-BN and HfO_2 stack is then employed as the gate dielectric heterostructure. In the previous reports, single-crystalline few-layer h-BN acquired through mechanical exfoliation is widely adopted due to its unique advantage of minimal surface dangling bonds or charge traps.[14,18] However, it is not suitable for our design here owing to the following reasons. Firstly, the uncontrollability in both thickness and shape of the exfoliated flake limits its practical application in a commercially viable device. Secondly, a nearly perfect crystal structure refers to the existence of minimal surface charge traps, but the lack of dangling bonds on the h-BN plane would deter the subsequent nucleation of high-quality dielectric films overgrown in atomic layer deposition (ALD). Even though the functionalization of 2D materials with remotely generated ozone[19] or metal oxide nanoparticle[20,21] has been demonstrated as a solution for the nonuniform ALD growth of high-κ dielectrics and being widely adopted, it unavoidably modifies the surface morphology and composition of 2D materials. In comparison, few-layer h-BN synthesized by chemical vapor deposition (CVD) is more compatible with current micro- or nanofabrication processes which enable the efficient integration of this fascinating material into future device applications. More importantly, the thickness and surface morphology of CVD h-BN can be controlled by the growth conditions. Meanwhile, the existence of atomic defects induced on the h-BN film surface during CVD process is expected to provide dangling bonds for the subsequent ALD process and as well exclude any harmful surface functionalization scheme. In addition, HfO_2 is employed as the high-κ dielectric in this study due to many desirable properties such as the high dielectric constant, large heat of formation and relatively large band gap.[22] The conventional mechanical exfoliation method is still employed to obtain high-quality channel materials such as MoS_2 and graphene, which is necessary to evaluate the device performance limitation. In general, the fabrication process is shown in **Figure 1**. Here, the CVD h-BN films are coated with poly(methyl methacrylate) (PMMA) and transferred to target substrates for further characterization as previously reported in the graphene transfer (see Experimental Section).[23] The corresponding optical microscope image and Raman spectroscopy are shown in Figure S1 in the Supporting Information. This conventional transfer process is employed due to its advantage in the minimized damage, such as lattice damage or bond break, to bottom channel materials. It is noted that since the exfoliated 2D material is inert to ALD reactions, it is essential that the h-BN overlayer is continuous and conformal on the channel material surface. Also, top-gated field-effect transistors (FETs) are fabricated to allow the individual operation of each device in integrated circuit as well as to further enhance the gate capacitance for better performance.

Specifically, the transistors with SiO_2/MoS_2/h-BN/HfO_2 stack are first fabricated to assess their interface quality. As presented in **Figure 2**a, the corresponding cross-sectional high-resolution transmission electron microscopy (HRTEM) image exhibits a uniform and compact interface between h-BN and HfO_2 without any gap and obvious defects. This is consistent with the measurement of surface roughness using atomic

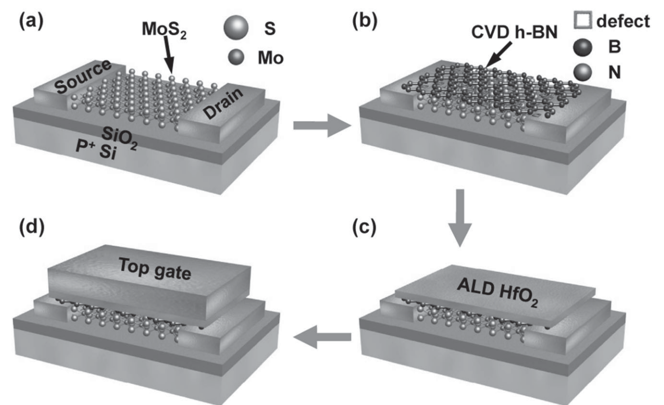

Figure 1. Schematic illustration of the fabrication of MoS_2 transistor with the h-BN/HfO_2 dielectric stack. a) Back-gated MoS_2 transistor with Cr/Au (5/50 nm) electrodes is first defined by electron beam lithography, followed by metal deposition and lift-off processes. b) The channel material is then covered by few-layer CVD h-BN, which aims to minimize the surface charge traps and optical phonon scattering at the channel/dielectric interface. At the same time, a large amount of atomic defects would be induced on the h-BN surface during CVD growth, in which these defect sites can supply sufficient dangling bonds for the subsequent ALD nucleation. c) A 16 nm thick HfO_2 is deposited by ALD to alleviate Coulombic scattering and to enhance the effective gate capacitance. d) Top-gated electrode of Ni/Au (15/50 nm) is finally defined to accomplish the device construction.

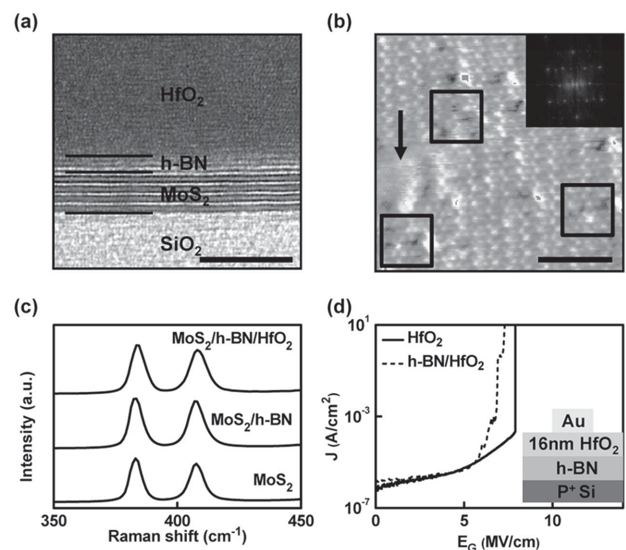

Figure 2. Structural and electrical properties of h-BN/HfO_2 dielectric heterostructure. a) Cross-sectional HRTEM image of a SiO_2/MoS_2/h-BN/HfO_2 stack with 16 nm thick ALD–HfO_2 on CVD h-BN. Scale bar is 5 nm. b) STM topographic images of crystal defects observed on the Cu-supported CVD h-BN sample. Type A defects (marked with arrow) indicate subsurface irregularities blanketed by h-BN. Type B defects (marked with box) designate atomic defects existed in the h-BN lattice. Scale bar is 2 nm. The inset shows a Fourier transform pattern of a region with defects. c) Raman spectra of the few-layer MoS_2 flake before and after h-BN deposition, followed by HfO_2 growth. d) The leakage current density (J) versus gate field (E_G) curves measured for capacitors fabricated with different dielectric structures. Inset gives the device schematic of the fabricated capacitor.

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force microscopy (see details in Figure S1 in the Supporting Information). This result differs from the previous report of island overgrowth of dielectrics onto exfoliated 2D crystal materials,[24] but is consistent with the report of Al_2O_3 deposited onto CVD h-BN directly.[25] These contradicting results can be attributed to the existence of massive atomic defects induced on the surface of h-BN during CVD process, as evidenced by scanning tunneling microscopic (STM) measurement (Figure 2b). The survey of this image reveals two categories of surface defects. Type A defects, like a mound (marked with arrow in Figure 2b), have an unperturbed h-BN structure that is akin to a blanket. These defects are due to irregularities in the interface layer between h-BN and the Cu substrate during the CVD process. In contrast, type B defects are atomic vacancies within the h-BN lattice and are accompanied by surface dangling bonds, in which these unsaturated bonds can facilitate the nucleation of HfO_2 during ALD process. By examining the Fourier transform of a selected region (Figure 2b inset), we can confirm its distinctive hexagonal lattice and lattice constant of 0.253 nm. At the same time, Figure 2c gives the Raman spectra of few-layer MoS_2 flake before and after the h-BN/HfO_2 deposition. There is no obvious change in Raman spectra among all structures, indicating that the h-BN/HfO_2 stack fabricated in the present dielectric engineering do not introduce any noticeable lattice damage or bond-disorder into the MoS_2 channel.

In order to evaluate the dielectric characteristic of h-BN/HfO_2 heterostructured stack and investigate the corresponding device performance, the capacitors are fabricated by depositing 16 nm thick HfO_2 on p+-Si substrates with and without the h-BN interlayer, respectively, with the schematic illustration as shown in the inset of Figure 2d. As compared with the pure HfO_2 dielectric, HfO_2 deposited with the h-BN interlayer displays a slight decrease in the breakdown field from 8 to 6.5 MV cm^{-1}; however, this value is already much better than that of using CVD h-BN alone as the top gate dielectric (1.5–2.5 MV cm^{-1}),[26] indicating a substantial improvement in the electrical reliability here. Also, the capacitance is measured at 1 MHz using Keithley 4200 with the typical device size of 100 µm × 100 µm. The extracted dielectric constant of CVD h-BN is found to be 0.5–1 (see details in Figure S2 in the Supporting Information). Notably, even if this value is smaller than that extracted from bulk materials, it is still consistent with previous theoretical prediction for few-layer 2D materials (≈1).[27,28]

For practical utilizations of this dielectric engineering, we have to first examine the impact of h-BN/HfO_2 dielectric heterostructure on the transport properties of 2D materials based devices. MoS_2 and graphene, which represent the thinnest possible manifestations of semiconductor materials integrated into logic and radio frequency applications,[29–32] respectively, are used as semiconductor channel materials here. Transfer length method (TLM) is employed for the deduction of contact resistance and extraction of carrier intrinsic mobility in the devices. Although the fitting method is more popular and extensively adopted in the graphene community due to its simplicity in the device fabrication,[14,17] characteristic in presupposing a constant mobility independent of the carrier density would make it overestimate the carrier mobility and being unsuitable for the accurate measurement.[33] Moreover, in order to eliminate the influence of water molecules which come from ambient moisture adsorbed on the surface of 2D materials and SiO_2 substrates, the pristine back-gated devices are heated at 250 °C for 4 h in a high vacuum chamber. A similar heating process is also performed for all devices after the h-BN transfer to drive off water molecules and residuals (see details in Experimental Section). All the measurements are then performed at 25 °C under high vacuum condition.

As depicted in **Figure 3**a, MoS_2 devices with varying channel lengths (0.3, 0.5, 1, and 2 µm) are fabricated. Here, few-layer (3–5 layers) MoS_2 are employed as the channel material to obtain high current density and mobility, meanwhile, to avoid degradation in current on/off ratio or sub-threshold slope (*SS*). The field-effect mobility (μ_{FE}) is extracted from devices of 2 µm channel length using the low-bias transconductance (g_m) measured in the transfer characteristics, $g_m = (dI_{ds})/(dI_{gs})|V_{ds}$, and the analytical expression, $\mu_{FE} = g_m(L_{ch}^2/C_{ox})(1/V_{ds})$, where L_{ch} = 2 µm is the device channel length and C_{ox} is the gate capacitance. Using the approximate back-gated unit-area capacitance value of 130 nF cm^{-2} for the 265 nm thick SiO_2 substrate and measured device parameters, an improved back-gated μ_{FE} value from 64 to 85 cm^2 V^{-1} s^{-1} is obtained after the h-BN/HfO_2 dielectric processing (Figure 3b). At the same time, Figure 3c illustrates the top-gated transfer characteristics recorded from the same device. The calculated top-gated μ_{FE} value is 88 cm^2 V^{-1} s^{-1} at V_{gs} = –0.2 V, together with an excellent sub-threshold slope SS = 78 mV dec^{-1}, which can be further improved through the reduction of dielectric thickness. In details, interface trap density (D_{it}) is employed to evaluate the interface quality using the equation,[34] $D_{it} = (C_i/q)((q/KT)(SS/\ln10)-1)$, where C_i is the unit-area capacitance of the top gate (Figure S2, Supporting Information), q is the electron charge and T is the measurement temperature. Using this equation, the D_{it} value is calculated to be 7 × 10^{11} cm^{-2} eV^{-1} which is better than our previously reported value for the MoS_2/Y_2O_3/HfO_2 stack,[21] indicating an improved interface quality employing the h-BN interlayer in this work. Using TLM (see details in Figure S3 in the Supporting Information), the contact resistance (R_c) at V_{gs} = –0.2 V is extracted to be 11.5 Ω·mm. Combining this value, the total resistance (R_{on}) of 76.9 Ω mm at V_{gs} = –0.2 V and L_{ch} = 2 µm, the drain voltage can be corrected to 0.85 V using the equation . Accordingly, a high intrinsic mobility of 104 cm^2 V^{-1} s^{-1} is then obtained, which is one of the highest room-temperature values for top-gated MoS_2 device reported so far. Similar behavior is also observed for other 10 MoS_2 devices and, importantly, we always measured a higher mobility after the h-BN/HfO_2 deposition as compared with the pristine devices. The output characteristics of back-gated and top-gated device are as well measured as given in Figure 3d–f, the increase in current after the dielectric deposition can be attributed to the reduced carrier scattering, with all these suggesting the high-quality ohmic-like contact and current saturation here.

A similar improvement in the mobility is also observed in monolayer graphene devices. **Figure 4**a shows the back-gated transfer characteristics of a monolayer graphene device with L_{ch} = 2 µm before and after the h-BN/HfO_2 deposition, respectively. The relatively narrow I_{ds}–V_{gs} curve near Dirac point provides a clear demonstration of suppressed long-range Coulombic scattering after the dielectric heterostructure

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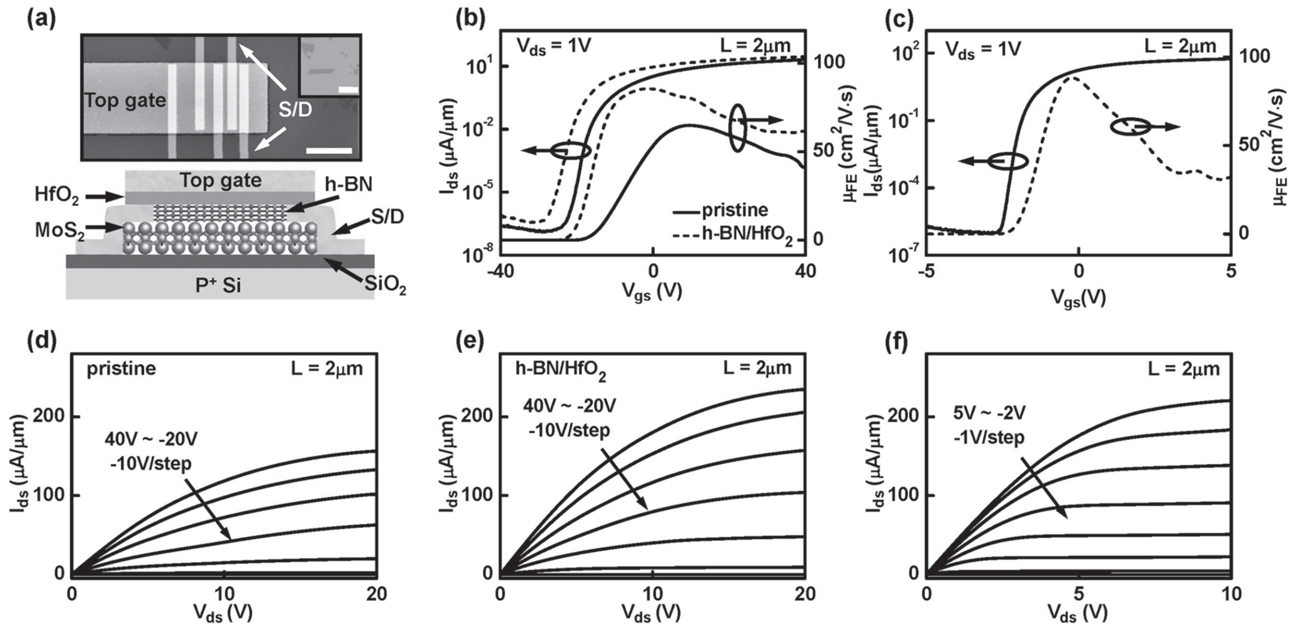

Figure 3. Electron transport in few-layer MoS_2 FETs. a) Illustrative schematic and SEM image of a top-gated MoS_2 FET with the h-BN/HfO_2 dielectric stack. Varied device channel lengths (i.e., 0.3, 0.5, 1, and 2 μm) are prepared to extract the contact resistance and intrinsic mobility. The complete gate-to-source or gate-to-drain overlapping is used to minimize the parasitic resistance. The upper inset shows the optical image of few-layer MoS_2 employed for the device fabrication. All the scale bars are 5 μm. b) Transfer characteristics and field-effect mobility of a back-gated MoS_2 FET before and after h-BN/HfO_2 transfer. c) Transfer characteristics and field-effect mobility of the same MoS_2 device configured with the top-gated geometry. d,e) Output characteristics of a back-gated MoS_2 FET before and after h-BN/HfO_2 transfer. f) Output characteristics of the same device configured with the top-gated geometry.

deposition as expected.[14,35] A little negative shift of Dirac point may be due to the transfer residues and/or n-doping induced by the overgrowth of h-BN.[36,37] In addition, the I_{ds} curve is more sublinear at the high gate bias after the dielectric stack is deposited. This can be associated with the decreased screening of the impurity potential by charge carriers,[35] which increases the carrier scattering for the lower conductivity at high carrier density. Using the same equation above, the extracted μ_{FE} value of the back-gated device is improved from 6300 to 8100 $cm^2\ V^{-1}\ s^{-1}$ after the h-BN/HfO_2 deposition. At a maximum g_m of 132 μS μm^{-1} (Figure 4b), the corresponding μ_{FE} value of top-gated device is calculated to be 7400 $cm^2\ V^{-1}\ s^{-1}$. Subtracting the contact resistance obtained by TLM (see details in Figure S4 in the Supporting Information), the corresponding intrinsic electron mobility can be further enhanced to 9700 $cm^2\ V^{-1}\ s^{-1}$; meanwhile, the top-gated device also exhibits a clear drain current saturation (Figure 4c), yielding a maximum output current density of 2.9 mA μm^{-1} and a minimum output conductance (g_{ds}) of 0.016 mS μm^{-1} in the saturation region (Figure S5, Supporting Information). Notably, the measured largest g_m is 0.92 mS μm^{-1} at L_{ch} = 2 μm and V_{ds} = 2 V. This way, the corresponding intrinsic gain (g_m/g_{ds}) is calculated to be 58, which is much larger than the previous reports with similar channel lengths.[38] This intrinsic gain is an important figure-of-merit in analog amplifiers, representing the theoretical maximum gain achievable by a single transistor.[39] In this case, this gain value can be further enhanced for a longer channel device, illustrating that our top-gated graphene devices are attractive for practical amplifier applications.

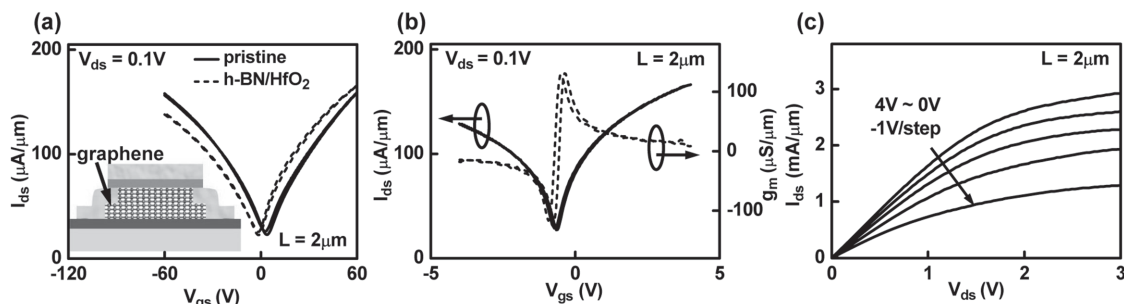

Figure 4. Electron transport in monolayer graphene FETs. a) Transfer characteristics of a back-gated graphene FET before and after h-BN/HfO_2 deposition. Inset shows the device schematic of the fabricated, top-gated graphene FET. b) Transfer characteristics and g_m of the same graphene device configured with the top-gated geometry. c) Output characteristics of the top-gated graphene FET.

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To shed light on the origin of this saturation behavior in our graphene transistors, we focus on a particular device displaying good saturation characteristics at the zero gate bias (Figure S6, Supporting Information). Interestingly, no clear current saturation is observed in the same device when the gate electrode is floated, suggesting that the current saturation observed here is probably due to the electrostatic pinch-off of the channel, rather than the velocity saturation of charge carriers associated with the phonon scattering.[40,41] Overall, the results obtained in this work using the h-BN/HfO_2 heterostructured dielectric stack can yield a dramatic improvement in the corresponding device performance as compared with other dielectric engineering methods, where the substantial performance degradation is typically acquired in top-gated operation. In any case, the mobility improvement here is slightly less than the previous reports using h-BN as the device substrate, probably due to the negative influence imposed by the underlying amorphous SiO_2 substrate. In addition, although the smaller lattice mismatch in the case of graphene/h-BN than MoS_2/h-BN, there is not any obvious difference observed. This is probably due to the disorder stack during transfer process.

Besides 2D semiconductor nanostructures, we further assess the feasibility of applying our h-BN/HfO_2 dielectric engineering scheme to conventional semiconductor heterostructures which have the favorable physical property of high-density 2D electron gas with high mobility in the III–V quantum well systems. For example, GaN-based HEMTs are promising candidates for the efficient operation in high-frequency power amplifiers and high-voltage power switches;[42,43] however, typical Schottky-barrier AlGaN/GaN HEMTs (SB–HEMTs) often feature a channel close to the polarized crystal surface, in which the corresponding carrier transport can be easily suffered from surface state induced adverse impact such as the current collapse.[44,45] Moreover, the high leakage current caused by the Schottky gate would further reduce the breakdown voltage, gate voltage swing and device reliability, in addition to increasing the static power dissipation. In general, in order to solve all these problems, a thin dielectric oxide layer is always introduced between the gate metal and the AlGaN barrier layer, leading to the improved device configuration of metal-oxide-semiconductor (MOS)–HEMTs;[46,47] as a result, surface traps at the AlGaN layer can be passivated and the gate leakage current can also be greatly suppressed. On the other hand, during the oxide dielectric deposition process, Ga–O bonds are formed on the AlGaN surface,[48–50] resulting in threshold voltage (V_{th}) instability and Fermi-level pinning at the AlGaN/dielectric interface. Recently, it is found that by inserting a 2 nm thick AlN interlayer with plasma enhanced ALD (PEALD) prior to the gate dielectric deposition, the low D_{it} value has been achieved in GaN-based MOS–HEMTs with small V_{th} hysteresis.[48,51] In this regard, we purposely employ our h-BN/HfO_2 dielectric heterostructure as the gate insulator here, since a high-quality interface can be readily obtained because of the atomically smooth surface of h-BN. Apart from that, the moderate ALD process is as well expected to prevent the inevitable lattice damage induced by plasma bombardment during PEALD processes.

Specifically, the AlGaN/GaN material structure used in this study includes a 22 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer, a 1 nm thick AlN interlayer, a 1.5 µm thick GaN buffer layer and a 100 nm thick AlN nucleation layer. Highly thermal conductive SiC substrate is employed to suppress the self-heating effect. **Figure 5**a shows the cross-sectional schematic and SEM image of the MOS–HEMT device here. The device fabrication consists of conventional FET fabrication steps. Briefly, ohmic contacts are first formed by evaporating a multilayered Ti/Al/Ni/Au stack followed by rapid thermal annealing at 850 °C for 30 s in a N_2 ambient. Then, the sample surface is treated with diluted HCl for 1 min at room temperature to remove the native oxide layer. After the h-BN transfer, a 16 nm thick HfO_2 is grown by ALD at 95 °C. Ni/Au (15/50 nm) gate electrode is finally done by thermal evaporation. The gate length (L) and width (W) are 1.5 and 100 µm, respectively. At the same time, SB–HEMTs with Ni/Au electrode and MOS–HEMTs with the single HfO_2 gate dielectric are as well prepared for the comparative study.

As depicted in the cross-sectional HRTEM image of AlGaN/h-BN/HfO_2 stack in Figure 5b, a high-quality h-BN interlayer is successfully inserted into the AlGaN/h-BN/HfO_2 stack. In addition, it is clear that the HfO_2 grown on h-BN is fully crystalline, which is quite different from ALD of HfO_2 on the metal oxide interfacial layer.[21] Further studies are required to clarify the crystallization mechanism. Figure 5c gives the transfer characteristics of different type of devices at V_{ds} = 10 V. The corresponding gate leakage curves are shown in Figure S7 in the Supporting Information. In contrast with SB–HEMTs, the negative V_{th} shift of MOS–HEMTs can be attributed to the increase of the barrier thickness. On the other hand, a significant reduction in g_m of MOS–HEMTs is observed for the ones without h-BN interlayer, but not for those with h-BN/HfO_2 stack. Without the h-BN interlayer, the reduced g_m value is mainly caused by the significant reduction of capacitance (Figure S8, Supporting Information). After the insertion of h-BN layer, the g_m value gets boosted. This is probably due to the improved interface quality and surface passivation effect which are expected to improve carrier transport. In this case, we prepare devices with L = 100 µm and W = 200 µm in order to evaluate the field-effect mobility at V_{ds} = 0.1 V. Using the extracted g_m and measured capacitance value, the μ_{FE} value of 2500 $cm^2 V^{-1} s^{-1}$ is obtained at low electric field for the h-BN inserted device, which is larger than that of SB–HEMTs (1600 $cm^2 V^{-1} s^{-1}$) and MOS–HEMTs without h-BN interlayer (2000 $cm^2 V^{-1} s^{-1}$). Output characteristics of the devices with 1.5 µm gate length are as well measured (Figure S9, Supporting Information). It is also worth to note that the maximum drain current of MOS–HEMTs with the h-BN interlayer is measured to be 1050 µA $µm^{-1}$, which is 56% larger than that of the SB–HEMT (674 µA $µm^{-1}$), with all these indicating the performance enhancement here. In the meantime, the current collapse of all devices are characterized by pulsed-IV measurements, where both V_{gs} and V_{ds} pulses are preset with the pulse width and period of 500 ns and 5 µs, respectively, along the gate/drain quiescent biases of −5/20 V. While SB–HEMTs exhibit the existence of current dispersion caused by surface traps in the gate-drain area, MOS–HEMTs can readily suppress the current collapse, demonstrating the outstanding resistance to current collapse for the devices with h-BN/HfO_2 dielectric heterostructure stack.

Furthermore, V_{th} instability induced by electron trapping/detrapping processes at the dielectric/AlGaN interface is a

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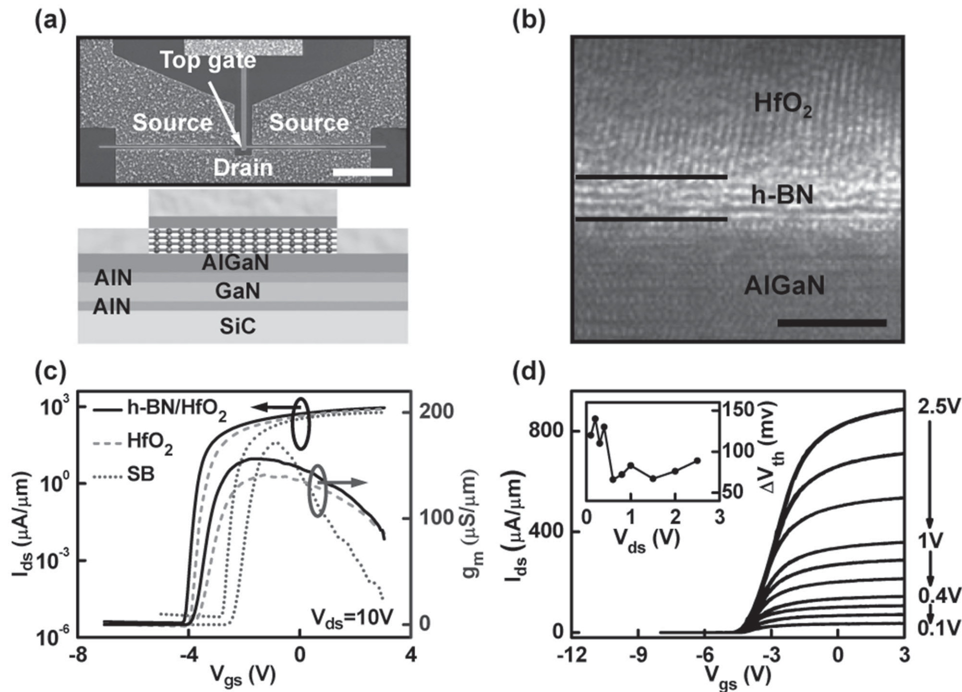

Figure 5. Electron transport in GaN-based HEMTs. a) Cross-sectional schematic and top-viewed SEM image of a MOS–HEMT. The scale bar is 50 µm. b) Cross-sectional HRTEM image of a AlGaN/h-BN/HfO_2 stack. The scale bar is 5 nm. c) Transfer characteristics and g_m of SB–HEMT and MOS–HEMTs. d) Pulse-mode transfer characteristics of the MOS–HEMT with h-BN interlayer in the linear region. The inset displays the V_{th} hysteresis varied with different applied V_{ds}.

critical issue in the GaN-based MOS–HEMT devices.[52,53] Conventional hysteresis curve can be characterized by dc-mode I_{ds}–V_{gs} measurement with a slow sweeping rate, which affords a sufficient time during the down-sweep process for electrons to be emitted from all shallow traps and part of deep traps. In this work, in order to avoid the underestimation of V_{th} shift (ΔV_{th}) induced by dc measurement, the sweep transfer characteristics are measured by pulsed I_{ds}–V_{gs} with various drain biases during the MOS–HEMT operation. In brief, the measurement here consists of an up-sweep process with the base voltage of −8 V and a down-sweep process with the base voltage of +3 V. The pulse width and period are maintained at 2 and 20 ms, respectively (Figure S10, Supporting Information). Also, the positive base voltage of +3 V in down-sweep is employed to fill up all interface trap states before each measurement point. The short pulse width of 2 ms is selected to aim for retaining all electrons trapped in interface states with the emission time constant larger than 2 ms. In contrast to MOS–HEMT devices with only the HfO_2 dielectric (Figure S10, Supporting Information), devices with the h-BN/HfO_2 stack show a smaller V_{th} shift (Figure 5d). This can be attributed to the prevention of the Ga–O bonding formation during ALD HfO_2 deposition by inserting the h-BN interlayer, which acts as an efficient oxygen diffusion barrier between HfO_2 and AlGaN due to its advantage in impermeability.[54] Also, the interface trap density can be estimated by the equation $D_{it} = C_i \cdot \Delta V_{th}/q$. Using the unit-area capacitance of HfO_2 and h-BN/HfO_2 (Figure S8, Supporting Information), the D_{it} value is calculated to be 0.3×10^{12} cm^{-2} and 2.8×10^{12} cm^{-2} for samples with and without h-BN interlayer, respectively. **Table 1** compiles a comparison of all extracted device parameters from all different type of devices studied in this work. Importantly, the improved D_{it} and SS values observed in all h-BN inserted MOS–HEMTs indicate that the existence of h-BN layer can effectively reduce the interface trap density. As a result, all these present the technological potency of this dielectric engineering using h-BN/HfO_2 stack as a gate insulator for the effective integration of high-performance GaN MOS–HEMTs that are highly desirable in power switching applications.

For the current atomically thin 2D semiconductor channel materials, the major achievement of corresponding carrier mobilities obtained to date are still far below than their theoretical intrinsic values. These degraded mobilities are mostly caused by Coulombic impurity scattering and surface optical phonon scattering induced from the underlying substrate. Among many approaches to enhance these mobility values, one simple solution is to enhance the crystal quality at the channel/dielectric interface for the fabricated 2D devices in order to alleviate all the other carrier scattering mechanisms. In this letter, we have demonstrated that h-BN/HfO_2 dielectric heterostructure stack can serve as an appealing gate insulator to suppress

Table 1. The comparison of field effect mobility and other electrical properties.

Dielectrics	μ_{FE} [cm^2 V^{-1} ·s^{-1}]	D_{it} [10^{12} cm^{-2}]	SS [mV dec^{-1}]
Schottky barrier	≈1600		67 ± 2
HfO_2	≈2000	2.8	80 ± 2
h-BN/HfO_2	≈2500	0.3	70 ± 2

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the above-mentioned carrier scatterings. Specifically, the high-performance top-gated transistors with h-BN/HfO_2 dielectrics have been fabricated with both graphene and MoS_2 as the 2D device channels. The obtained transistors exhibit both distinct mobility enhancement and superior gate control. Apart from the 2D channel materials, we as well integrate the h-BN/HfO_2 stack into the GaN-based MOS–HEMTs for the performance enhancement due to the improved channel/dielectric interface quality. In conclusion, this unique dielectric design of h-BN/HfO_2 heterostructure stack represents a significant improvement over the previous efforts, which will hopefully drive the further advancement of MOSFETs.

Experimental Section

h-BN Synthesis: Solid ammonia borane (97%) was purchased from Alfa Aesar. Cu foils were firstly annealed in Ar/H_2 (200/50 sccm) environment for 6 h, and then they were loaded into 1 in. diameter CVD fused quartz tube. Prior to h-BN growth, the CVD quarter tuber was pumped to ≈10 Pa, then Ar_2 flow rate was switched to 40 sccm and the pressure was maintained at 30–40 Pa by mechanical pumping. Once the desired growth temperature (1000 °C) was obtained, solid ammonia borane precursor placed in a quartz boat was heated to growth temperature (90 °C) by a heating belt for the decomposition of the source. After certain period of growth time (70 min), the h-BN monolayer film was synthesized.

ALD Growth of HfO_2: ALD of HfO_2 was performed at 95 °C using tetrakis(dimethylamino)hafnium (TDMAH) and H_2O precursors. The TDMAH precursor source was heated to 90 °C while the H_2O source was kept at room temperature. The carrier and purge gas was high purity Ar_2 with a flow rate of 30 sccm. The pulse time for TDMAH and H_2O were 0.03 and 0.02 s, respectively. The post TDMAH pulse purge was with Ar_2 for 120 s and the post H_2O purge was with Ar_2 for 100 s. All these process conditions would result in a growth rate of 1.2 Å/cycle.

CVD h-BN Transfer: The as-grown h-BN film on Cu foil was spin coated with PMMA at 3000 rpm for 1 min, which was then cured at 180 °C for 5 min. The Cu substrate was etched away by an aqueous solution of iron nitrate (0.05 g mL^{-1}) over a period of 12 h. To remove the residual iron particles which came from the copper etchant, the PMMA/h-BN stack was floated on 10% HCl for 1 h. Subsequently, the film was washed with deionized water and placed on the target substrates and dried at 90 °C. In the end, PMMA was removed by acetone.

STM Characterization: The STM system was an ultrahigh vacuum single-probe scanning probe microscope (USM-1500) from UNISOKU. All STM measurements were performed at 78 K and the images were taken in a constant-current scanning mode. The STM tips were obtained by chemical etching from a wire of Pt(80%) Ir(20%) alloys. Lateral dimensions observed in the STM images were calibrated using a standard graphene lattice as well as a Si (111)–(7 × 7) lattice.

Device Fabrication and Electrical Measurements: Few-layer MoS_2 and monolayer graphene were mechanically exfoliated from bulk crystals and transferred to the precleaned highly doped p-type silicon substrates with a thermally grown 265 nm thick SiO_2 layer. Then the substrates were spin coated with MMA and PMMA, and the EBL (JEOL 6510 with NPGS) was employed to define the source and drain pattern followed by metal evaporation and lift-off processes. Here, Cr/Au (5/50 nm) and Ni/Au (5/50 nm) were deposited as contact electrode to ensure high-quality ohmic-like contact in MoS_2 and graphene devices, respectively. After h-BN transfer, the pristine back-gated devices were heated at 250 °C for 4 h in an ultrahigh vacuum chamber to drive off water molecules and residual. A 16 nm thickness HfO_2 was subsequently deposited by ALD which was ensured by AFM and ellipsometry. In order to avoid overestimated results induced by capacitive coupling between the top- and back-gates, the deposition of top-gated electrode (15 nm Ni/50 nm Au) was delayed until all measurements in back-gated configuration were finished. Electrical characterizations were carried out with the Lake Shore TTPX Probe Station and Agilent 4155C Semiconductor Parameter Analyzer. Capacitance-voltage characteristics were measured with Keithley 4200. AFM imaging was performed by Bruker Multimode 8.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] K. Nomura, A. H. MacDonald, *Phys. Rev. Lett.* **2007**, *98*, 076602.
[2] E. H. Hwang, S. Adam, S. Das Sarma, *Phys. Rev. Lett.* **2007**, *98*, 186806.
[3] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, M. S. Fuhrer, *Nat. Nanotechnol.* **2008**, *3*, 206.
[4] M. Ishigami, J. H. Chen, W. G. Cullen, M. S. Fuhrer, E. D. Williams, *Nano Lett.* **2007**, *7*, 1643.
[5] M. I. Katsnelson, A. K. Geim, *Philos. Trans. R. Soc. A* **2008**, *366*, 195.
[6] S. V. Morozov, K. S. Novoselov, M. I. Katsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, A. K. Geim, *Phys. Rev. Lett.* **2008**, *100*, 016602.
[7] S. Fratini, F. Guinea, *Phys. Rev. B* **2008**, *77*, 195415.
[8] X. Du, I. Skachko, A. Barker, E. Y. Andrei, *Nat. Nanotechnol.* **2008**, *3*, 491.
[9] K. I. Bolotin, K. J. Sikes, J. Hone, H. L. Stormer, P. Kim, *Phys. Rev. Lett.* **2008**, *101*, 096802.
[10] D. Jena, A. Konar, *Phys. Rev. Lett.* **2007**, *98*, 136805.
[11] A. Konar, T. Fang, D. Jena, *Phys. Rev. B* **2010**, *82*, 115452.
[12] N. Ma, D. Jena, *Phys. Rev. X* **2014**, *4*, 011043.
[13] H. Hirai, H. Tsuchiya, Y. Kamakura, N. Mori, M. Ogawa, *J. Appl. Phys.* **2014**, *116*, 083703.
[14] C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, J. Hone, *Nat. Nanotechnol.* **2010**, *5*, 722.
[15] G.-H. Lee, Y.-J. Yu, X. Cui, N. Petrone, C.-H. Lee, M. S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, J. Hone, *ACS Nano* **2013**, *7*, 7931.
[16] K. Kim, J.-Y. Choi, T. Kim, S.-H. Cho, H.-J. Chung, *Nature* **2011**, *479*, 338.
[17] D. B. Farmer, H.-Y. Chiu, Y.-M. Lin, K. A. Jenkins, F. Xia, P. Avouris, *Nano Lett.* **2009**, *9*, 4474.

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[18] H. Wang, T. Taychatanapat, A. Hsu, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero, T. Palacios, *IEEE Electron Device Lett.* **2011**, *32*, 1209.
[19] B. Lee, G. Mordi, M. J. Kim, Y. J. Chabal, E. M. Vogel, R. M. Wallace, K. J. Cho, L. Colombo, J. Kim, *Appl. Phys. Lett.* **2010**, *97*, 043107.
[20] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, S. K. Banerjee, *Appl. Phys. Lett.* **2009**, *94*, 062107.
[21] X. Zou, J. Wang, C.-H. Chiu, Y. Wu, X. Xiao, C. Jiang, W.-W. Wu, L. Mai, T. Chen, J. Li, J. C. Ho, L. Liao, *Adv. Mater.* **2014**, *26*, 6255.
[22] B. H. Lee, L. G. Kang, R. Nieh, W. J. Qi, J. C. Lee, *Appl. Phys. Lett.* **2000**, *76*, 1926.
[23] X. Li, Y. Zhu, W. Cai, M. Borysiak, B. Han, D. Chen, R. D. Piner, L. Colombo, R. S. Ruoff, *Nano Lett.* **2009**, *9*, 4359.
[24] S. McDonnell, B. Brennan, A. Azcatl, N. Lu, H. Dong, C. Buie, J. Kim, C. L. Hinkle, M. J. Kim, R. M. Wallace, *ACS Nano* **2013**, *7*, 10354.
[25] Q. Han, B. Yan, T. Gao, J. Meng, Y. Zhang, Z. Liu, X. Wu, D. Yu, *Small* **2014**, *10*, 2293.
[26] K. K. Kim, A. Hsu, X. Jia, S. M. Kim, Y. Shi, M. Dresselhaus, T. Palacios, J. Kong, *ACS Nano* **2012**, *6*, 8583.
[27] J.-H. Choi, P. Cui, H. Lan, Z. Zhang, *Phys. Rev. Lett.* **2015**, *115*, 066403.
[28] P. Cudazzo, I. V. Tokatly, A. Rubio, *Phys. Rev. B* **2011**, *84*, 085406.
[29] B. Radisavljevic, M. B. Whitwick, A. Kis, *ACS Nano* **2011**, *5*, 9934.
[30] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong, T. Palacios, *Nano Lettt* **2012**, *12*, 4674.
[31] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, X. Duan, *Proc. Natl. Acad. Sci. USA* **2012**, *109*, 11588.
[32] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, X. Duan, *Nature* **2010**, *467*, 305.
[33] H. Zhong, Z. Zhang, H. Xu, C. Qiu, L.-M. Peng, *AIP Adv.* **2015**, *5*, 057136.
[34] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **2011**, *6*, 147.
[35] C. Jang, S. Adam, J. H. Chen, D. Williams, S. Das Sarma, M. S. Fuhrer, *Phys. Rev. Lett.* **2008**, *101*, 146805.
[36] W. Gannett, W. Regan, K. Watanabe, T. Taniguchi, M. F. Crommie, A. Zettl, *Appl. Phys. Lett.* **2011**, *98*, 242105.
[37] L. Kong, C. Bjelkevig, S. Gaddam, M. Zhou, Y. H. Lee, G. H. Han, H. K. Jeong, N. Wu, Z. Zhang, J. Xiao, P. A. Dowben, J. A. Kelber, *J. Phys. Chem. C* **2010**, *114*, 21618.
[38] J. Bai, L. Liao, H. Zhou, R. Cheng, L. Liu, Y. Huang, X. Duan, *Nano Lett.* **2011**, *11*, 2555.
[39] F. Schwierz, *Nat. Nanotechnol.* **2010**, *5*, 487.
[40] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, K. L. Shepard, *Nat. Nanotechnol.* **2008**, *3*, 654.
[41] M. Freitag, M. Steiner, Y. Martin, V. Perebeinos, Z. Chen, J. C. Tsang, P. Avouris, *Nano Lett.* **2009**, *9*, 1883.
[42] U. K. Mishra, L. Shen, T. E. Kazior, Y.-F. Wu, *Proc. IEEE* **2008**, *96*, 287.
[43] N. Ikeda, Y. Niiyama, H. Kambayashi, Y. Sato, T. Nomura, S. Kato, S. Yoshida, *Proc. IEEE* **2010**, *98*, 1151.
[44] R. Vetury, N. Q. Q. Zhang, S. Keller, U. K. Mishra, *IEEE Trans. Electron Devices* **2001**, *48*, 560.
[45] G. Koley, V. Tilak, L. F. Eastman, M. G. Spencer, *IEEE Trans. Electron Devices* **2003**, *50*, 886.
[46] C. Liu, E. F. Chor, L. S. Tan, *Semicond. Sci. Technol.* **2007**, *22*, 522.
[47] Y. Yue, Y. Hao, J. Zhang, J. Ni, W. Mao, Q. Feng, L. Liu, *IEEE Electron Device Lett.* **2008**, *29*, 838.
[48] S. Huang, Q. Jiang, S. Yang, C. Zhou, K. J. Chen, *IEEE Electron Device Lett.* **2012**, *33*, 516.
[49] K. C. Mishra, P. C. Schmidt, S. Laubach, K. H. Johnson, *Phys. Rev. B* **2007**, *76*, 035127.
[50] C. L. Hinkle, M. Milojevic, B. Brennan, A. M. Sonnet, F. S. Aguirre-Tostado, G. J. Hughes, E. M. Vogel, R. M. Wallace, *Appl. Phys. Lett.* **2009**, *94*, 162101.
[51] S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, M. Wang, K. J. Chen, *IEEE Electron Device Lett.* **2014**, *35*, 723.
[52] T.-E. Hsieh, E. Y. Chang, Y.-Z. Song, Y.-C. Lin, H.-C. Wang, S.-C. Liu, S. Salahuddin, C. C. Hu, *IEEE Electron Device Lett.* **2014**, *35*, 732.
[53] S. Yang, S. Huang, M. Schnee, Q.-T. Zhao, J. Schubert, K. J. Chen, *IEEE Trans. Electron Devices* **2013**, *60*, 3040.
[54] X. Zheng, M. Zhang, X. Shi, G. Wang, L. Zheng, Y. Yu, A. Huang, P. K. Chu, H. Gao, W. Ren, Z. Di, X. Wang, *Adv. Funct. Mater.* **2015**, *25*, 1805.

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