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Anti-Ambipolar Heterojunctions: Materials, Devices, and Circuits

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Anti-ambipolar heterojunctions are vital in constructing high-frequency oscillators, fast switches, and multivalued logic (MVL) devices, which hold promising potential for next-generation integrated circuit chips and telecommunication technologies. Thanks to the strategic material design and device integration, anti-ambipolar heterojunctions have demonstrated unparalleled device and circuit performance that surpasses other semiconducting material systems. This review aims to provide a comprehensive summary of the achievements in the field of anti-ambipolar heterojunctions. First, the fundamental operating mechanisms of anti-ambipolar devices are discussed. After that, potential materials used in anti-ambipolar devices are discussed with particular attention to 2D-based, 1D-based, and organic-based heterojunctions. Next, the primary device applications employing anti-ambipolar heterojunctions, including anti-ambipolar transistors (AATs), photodetectors, frequency doublers, and synaptic devices, are summarized. Furthermore, alongside the advancements in individual devices, the practical integration of these devices at the circuit level, including topics such as MVL circuits, complex logic gates, and spiking neuron circuits, is also discussed. Lastly, the present key challenges and future research directions concerning anti-ambipolar heterojunctions and their applications are also emphasized.

1. Introduction

The rapid advancement of information and communication technologies, including artificial intelligence (AI), big data, and the Internet of Things (IoT), has ignited a transformative revolution in our daily lives.[1,2] It is not surprising that these transformative applications have created a tremendous demand for exponentially increasing computation and memory capacities.[3,4] As an example, if the demand for computational power and data storage continues to grow at its current pace, it is projected that the total energy consumption of the binary von Neumann computing architecture, based on complementary metal-oxide-semiconductor (CMOS) technology, could reach ≈10^{27} joules by 2040.[5] This staggering amount of energy consumption would undoubtedly surpass the anticipated global energy production levels.

The traditional CMOS-based von Neumann architecture is a stored-program system with separated memory and processing units designed to deal with binary information.[6,7] Over the years, computer components have undergone significant evolution to meet the increasing demands of upgraded workloads. For instance, processor speeds have significantly increased, and memory capacities have improved, enabling the storage of more intensive data in less physical space. However, in contrast to these advancements, the transfer rates between the processor and memory have only made modest improvements. Consequently, the processor often remains idle for extended periods as it awaits data retrieval from memory, a phenomenon commonly referred to as the von Neumann bottleneck. Researchers have made numerous attempts to tackle the issue of the von Neumann bottleneck through various approaches.[6] An effective approach involves transitioning from binary to multivalued logic operations, facilitating a faster processor, enabling expedited memory access, and enhancing overall information processing efficiency.[8–11]

Conventional CMOS technology uses complementary p-type and n-type unipolar transistors to construct integrated circuits (IC) for realizing logic functions.[12] These complementary technologies commonly utilize extrinsic doping processes, such as ion implantation and thermal diffusion, to achieve p-type or n-type unipolar semiconductors.[13] This doping process adds difficulties to device fabrication and circuit design. In contrast, anti-ambipolar transistors (AATs) exhibit a unique differential transconductance (or resistance) characteristic under positive/negative gate bias. This characteristic enables them to achieve enhanced data processing capabilities within a single device, resulting in significant circuit design simplification and reduced power consumption.[9,10] Building upon anti-ambipolar heterojunctions, recent advancements have revealed the potential of multivalued logic (MVL) devices, including ternary and

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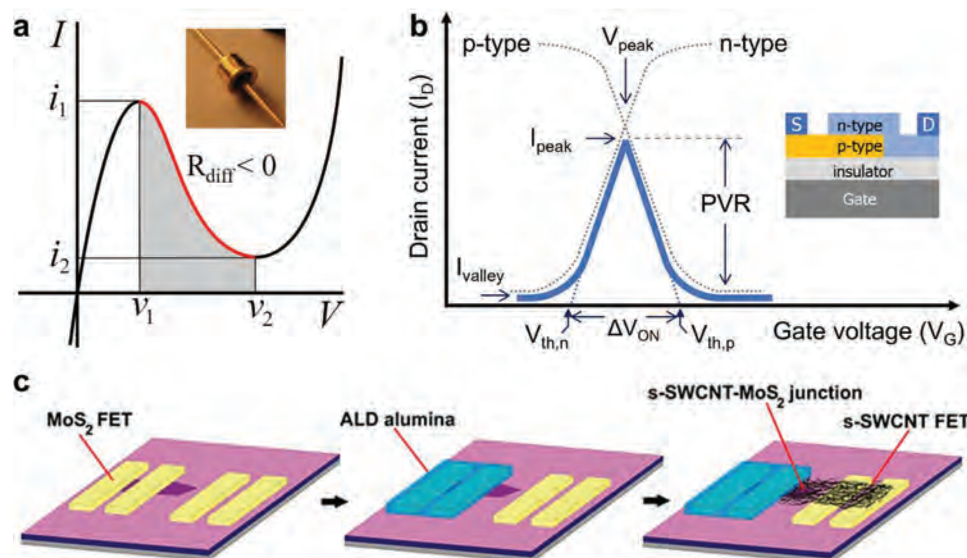

Figure 1. Esaki diodes and AATs. a) Typical NDR behavior and (inset) photograph of the two-terminal tunnel diode. b) Typical NDT behavior and (inset) device architecture of three-terminal transistors based on anti-ambipolar heterojunctions.[20] c) Fabrication process of anti-ambipolar heterojunctions based on p-SWCNTs and n-MoS_2.[21] a) Reproduced with permission. Copyright, Creative Commons CC0 1.0. b) Reproduced with permission.[20] Copyright 2018, American Chemical Society. c) Reproduced with permission.[21] Copyright 2013, PNAS.

quaternary logic gates, as promising architectures to surpass the fundamental bit limit.[8,11,14,15] Anti-ambipolar heterojunctions offer the possibility of achieving higher data storage density and facilitating the development of more powerful logic devices and circuits.

Since the 2010s, anti-ambipolar heterojunctions based on 2D layered materials and organic film semiconductors have been intensively studied. For instance, MVL circuits based on organic AATs by integrating two types of organic materials were demonstrated to show three different logic states most recently.[16] Besides, 2D materials and their heterostructures, e.g., MoS_2/WSe_2 heterojunctions and black phosphorus/MoS_2 heterojunctions,[17,18] were also used to construct ternary inverters, showing decent switching gains below 10. To bypass the limited resistance-capacitance time constant, high energy dissipation, and carrier concentration mismatching, the mixed-dimensional full-vdW 1D/2D heterostructures were proposed to realize the high-performance frequency doubling and MVL circuits.[19] Although anti-ambipolar heterojunctions are promising for high calculation capacity and low-power consumption, challenges remain in the area of material selection, fundamental physics, device construction, circuit integration, etc.

This review aims to provide a comprehensive overview of the recent advancements in anti-ambipolar heterojunctions, covering the areas of materials, devices, and circuits. We begin by examining the fundamental operating mechanisms of anti-ambipolar devices, followed by a discussion on potential materials, e.g., 2D-based, 1D-based, and organic-based heterojunctions. Then, the primary device applications based on anti-ambipolar heterojunctions, such as AATs, photodetectors, and frequency doublers, are covered. Additionally, we highlight the integration of these devices into macroscale circuits, including MVL circuits, complex logic gates, and spiking neuron circuits. Finally, we discuss future research trends and potential target applications associated with anti-ambipolar heterojunctions.

2. Fundamentals

2.1. From Esaki Diodes to Anti-Ambipolar Transistors

In 1958, Esaki first uncovered the phenomenon of negative differential resistance (NDR) in heavily doped germanium p-n junctions, which had a thickness of ≈15 nm.[22] In contrast to the I-V characteristics of a conventional diode, a tunnel diode exhibits an N-shaped NDR region during forward biasing. Beyond the critical peak voltage, the two-terminal Esaki diodes undergo a sudden current decrease, leading to a change in differential resistance (defined as $R_{diff} = dI/dV$) from positive to negative, which arises from the quantum-mechanical tunneling through the potential energy barrier (**Figure 1**a). Exploiting this unique behavior, tunnel diodes find application as the foundation for oscillators, amplifiers, and switching devices.[23] Subsequently, two-terminal devices utilizing different operating principles have been proposed to induce NDR behavior, including resonant tunneling diodes, Gunn diodes, and molecular-junction devices. The nonlinearity of electrical behavior observed in Esaki diodes also inspired intensive research into developing new types of electronic devices, while a similar NDR tunneling phenomenon has been uncovered in various emerging materials, such as graphene, black phosphorus (BP), metal-organic framework (MOF), and transition metal dichalcogenides (TMDC), etc.[24–27] Nevertheless, the intricate fabrication processes required for these tunneling devices have posed challenges to their practical implementation within the CMOS technology era.

In addition to two-terminal diode devices, extensive research has been conducted on the three-terminal transistor architecture as an alternative approach to achieve negative differential

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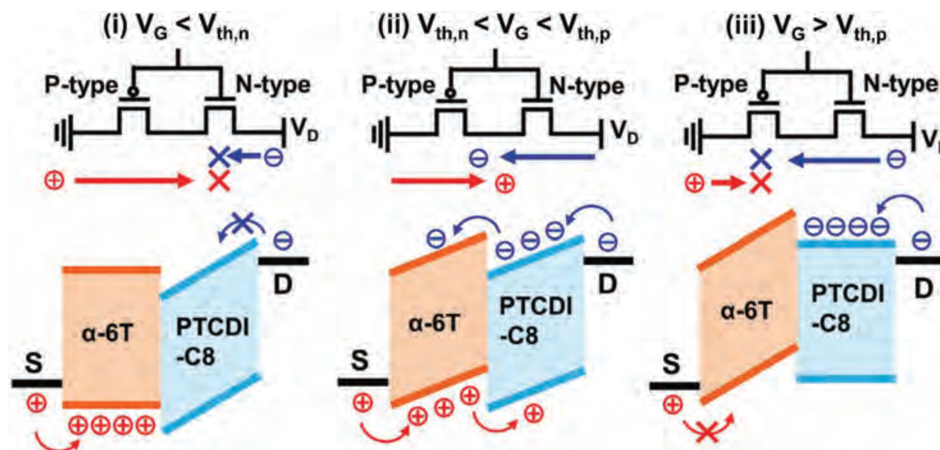

Figure 2. Carrier conduction mechanism of AATs with different gate voltages.[32] Reproduced with permission.[32] Copyright 2022, Wiley-VCH GmbH.

transconductance (NDT) behavior. The AATs employ the unique three-terminal transistor configuration made by anti-ambipolar heterojunctions. Within AATs, the n-type and p-type semiconductor films partially overlap in the middle of the channel region and connect separately to their respective electrodes. Anti-ambipolar heterojunctions possess the capability of transporting both electrons and holes, and the type of carriers injected is determined by the applied bias voltages. Consequently, the transfer curve displays a distinct Λ-shaped pattern (Figure 1b), switching between n-type and p-type characteristics at a specific gate bias voltage. At this turning point, the differential transconductance (defined as $g_m = dI_D/dV_G$) undergoes a transition from positive to negative. More importantly, the AATs, generally possessing planar device structure and operating at room temperature, are suitable for practical applications, which will be discussed in detail later. In recent years, we have observed the rapid development of AATs, summarized in several review articles focusing on 2D-based materials or organic-based materials.[9,28–31]

2.2. Carrier Transport Mechanisms

The combination of p-type semiconducting single-walled carbon nanotubes (SWCNTs) and n-type monolayer molybdenum disulfide (MoS_2) was used to create the first AAT device in a pioneering study (Figure 1c).[21] At the time of its development, the device was referred to as a gate-tunable pn-heterojunction diode, consisting of Au(source)/MoS_2(n-type)/CNTs(p-type)/Au(drain) layers on the dielectric layers. The p-n diode exhibited typical rectification characteristics, and more importantly, the rectification curves could be adjusted by applying V_G, leading to the formation of Λ-shaped transfer curves. Afterward, gate-tunable anti-ambipolar heterojunctions have been reported utilizing a wide range of materials, including organic and oxide thin films, one-dimensional (1D) nanowires, and two-dimensional (2D) layered materials, individually or in combination.

The AATs combine the p-channel and n-channel on the same substrate, which has a topological resemblance to CMOS circuits. Kobashi et al. recognized a resemblance between the Λ-shaped transfer curve observed in organic p-n heterojunction AATs and the shoot-through current observed in conventional CMOS inverters.[33] They demonstrated that the Λ-shaped curve, indicative of a spiky electrical current, occurs within a specific range of gate bias voltage during the transition between p-FET and n-FET operation. **Figure 2** depicts the corresponding carrier flow through simplified energy-level diagrams.[33] In the low V_G range ($V_G < V_{th,\,n}$), I_D was inhibited due to the n-channel being off-state, despite hole injection in the p-channel. In the middle V_G range ($V_{th,\,n} < V_G < V_{th,\,p}$), both p- and n-channels were simultaneously in the on-state, allowing the I_D to flow. Similarly, in the high V_G range ($V_G > V_{th,\,p}$), I_D was again suppressed as the p-channel switched off, even though the n-channel remained active. In general, achieving an appropriate energy-level offset between the p- and n-type materials is crucial for generating the Λ-shaped transfer curve.

The finite-element simulations successfully reproduced the gate-tunable operations of experimental AATs by analyzing the carrier transport mechanism, considering factors such as drift or diffusion, as well as the depletion or accumulation of holes and electrons.[34] Several key parameters were fitted to simulate this, including device geometries (channel lengths, widths, and thickness) and material properties (carrier mobility, carrier concentration, semiconductor band structures, dielectric constants of gate insulators, and work function of source/drain electrodes). It should be noted that these results were obtained through interface and geometry engineering from a general perspective. However, further in-depth investigations can be undertaken in the future.

2.3. Key Parameters

For AATs, their key parameters are peak voltage (V_{peak}), peak-to-valley ratio (PVR), and on-state bias range (ΔV_{ON}). A typical Λ-shaped transfer curve for AATs shows an increase in drain current (I_D) at the initial stages of gate bias voltage (V_G) application, followed by a decrease above a certain V_G (i.e., V_{peak}). At this peak, the corresponding transconductance values change from positive to negative. The V_{peak} is defined as the operation voltage of AATs, which should be as low as possible. The geometrical regulations

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of overlapping channel regions of anti-ambipolar heterojunctions can have a crucial impact on modifying the shape and position of the peaks, leading to excellent switching behavior.[35]

The PVR is defined as the ratio of maximum (I_{peak}) to minimum (I_{valley}) drain currents. Achieving high PVR and room temperature operation has presented challenges for conventional two-terminal NDR devices due to their typical requirement of cryogenic temperatures. For example, the Esaki diode achieved a PVR of 63 at cryogenic temperatures, but its PVR decreased to 30 at room temperature.[36] The presence of defects at the heterointerface is one of the reasons behind the diode's poor performance. The necessity for low operating temperatures and inadequate PVR have posed challenges in the development of practical devices and circuits. Compared to two-terminal diode devices, three-terminal AAT devices have shown a notable enhancement in PVR, typically by 2–3 orders of magnitude. Specifically, three-terminal AATs based on anti-ambipolar 2D materials or organics heterojunctions have significantly improved PVRs to $\approx 10^5$ while operating at room temperature.

The difference between the on-set voltage and off-set voltage defines the on-state bias range (ΔV_{ON}), which is initially dominated by the threshold voltages of the n-channel ($V_{th,\,n}$) and p-channel ($V_{th,\,p}$) semiconductors, respectively. A narrow ΔV_{ON} is desirable for achieving sharp switching, while an appropriately chosen ΔV_{ON} is necessary for designing high-performance logic circuits. In the case of organic anti-ambipolar heterojunctions, the transfer curve at the anti-electron regime is often significantly higher compared to the anti-hole regime, primarily because organic semiconductors typically exhibit low electron concentration and low electron mobility. In this regard, using semiconductors that possess balanced electron and hole mobilities has the potential to result in a more symmetric AAT transfer curve characterized by comparable positive and negative transconductance (g_m) and narrow ΔV_{ON}.

The effective control of V_{peak} and ΔV_{ON} in AATs can also be achieved by incorporating carrier injection layers at the interfaces of the semiconductor channel and metal electrodes. For example, a MoO_3 (Cs_2CO_3) thin film can function as a hole (electron) injection layer to lower the V_{th} of the p- (n-) FET.[20] Recently, Kobashi et al. successfully reduced V_{peak} by inserting Cs_2CO_3 films under the source/drain contact electrodes of AATs. MoO_3 (Cs_2CO_3) is well known as a high (low) work function material generally used in the surface charge transfer doping process.[37] In line with this thinking, some transition metal oxides with high work functions (6.8–7 eV), such as WO_3, CrO_3, and V_2O_5, could be utilized as hole injection layers, whilealkali metals with low work functions (2.3–2.9 eV), such as K and Li, could be used as electron injection layers. Alongside electrode contact engineering, the film thickness of the semiconductor channel also significantly impacts the performance of AATs, as confirmed by finite-element simulations.[38,39] These studies reveal that device design and fabrication could be utilized to boost the AATs performance, which will be discussed in the later section.

2.4. Carrier Transport Paths

Two potential carrier transport paths through the anti-ambipolar pn-heterojunction exist: the vertical interface and the lateral edge (**Figure 3a**). Controlled experiments were carried out by manipulating the organic device geometries to clarify this transport path. These experiments demonstrated that altering the overlapped pn-heterojunction length (ΔL; changing from 50, 150, to 250 µm) had a negligible effect on the AAT characteristics (including V_{peak} and I_{peak}) of organic p-type 6T/n-type PTCDI-C8 heterojunctions.[40] This finding may rule out the possibility of the vertical interface serving as a carrier transport pathway in organic AATs. In a compact modeling simulation, when no overlapped heterojunction length ($\Delta L = 0$) was considered at the lateral edge junction, the experimental anti-ambipolar behaviors were still successfully reproduced over a wide voltage range.[34,41] Based on these findings, the researchers concluded that the transport of both electrons and holes occurs through the lateral edge junction, which is influenced by the junction energy barrier and the penetration of minority carriers.

Another potential carrier transport mechanism explored is band-to-band tunneling through the vertical heterointerface (Figure 3b).[42] For instance, in cross-bar anti-ambipolar p-n heterojunctions based on TMDCs, Λ-shaped transfer curves were obtained despite the presence of only a vertical interface.[39,43] Gaining a comprehensive understanding of the carrier transport mechanism in anti-ambipolar heterojunctions is crucial. Besides, these analyses also suggest that creating a highly ordered junction is essential for optimizing AATs performance in the future.[44] Overall, the carrier transport mechanisms or paths of anti-ambipolar heterojunctions vary depending on the materials used, as reported in the literature. In most cases, 2D materials rely mainly on band-to-band vertical tunneling, while organic semiconductors most rely on drift-diffusion transport or short-through current in the lateral direction.

2.5. Characterization and Analysis Techniques

Since the engineering of anti-ambipolar heterojunctions offers the possibility to manipulate electrical transport properties, various characterization and analysis techniques can be employed to investigate these nanojunctions (**Table 1**).

As the band structure alignment process occurs, the electrical transport properties of heterojunctions experience notable alterations. Techniques such as junction diode and field-effect transistor (FET) measurements can be employed to characterize band structure engineering. Due to the rich knowledge accumulation on the related electrical characterization/analysis, this is the primary research method for an anti-ambipolar heterojunction study. Recently, temperature-dependent FET measurements (from 93 to 293 K) were employed as a well-established tool to exploit the underlying fundamental charge-transport mechanisms in organic DNTT/ PTCDI-C13 AATs.[35]

The electronic states and energy bands of semiconductors are closely tied to their optical properties. Hence, non-contact and non-destructive techniques such as Raman spectroscopy and photoluminescence (PL) spectroscopy can be employed to qualitatively assess the impact of band structure engineering on heterojunctions.[15] For instance, the fluorescence mapping and Raman mapping across the AATs heterojunction could indicate the junction edge and charge transfer process.[45,46] Charge separation-induced PL quenching of both heterojunction

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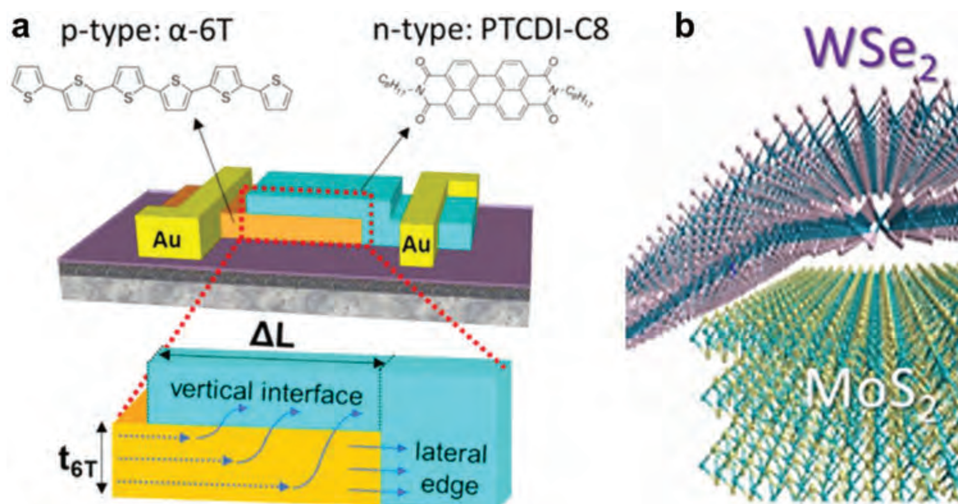

Figure 3. Carrier transport paths. a) Device structures and cross-sectional illustration of organic anti-ambipolar transistors.[40] b) 3D schematic illustration of the vertical WSe_2/MoS_2 heterojunctions.[17] a) Reproduced with permission.[40] Copyright 2018, American Chemical Society. b) Reproduced with permission.[17] Copyright 2016, American Chemical Society.

components was observed in type-II $InSe/C_{70}$ heterojunction, which is also supported by ultrafast transient absorption and reflection spectroscopy.[47]

Photoemission spectroscopy (PES) measurements are widely employed characterization techniques for investigating the electronic structures of semiconductors and their heterojunctions. The PES techniques involve the application of the photoelectric effect, where the electrons are emitted from solids by irradiation of a monochromatic photon beam. X-ray photoemission spectroscopy (XPS) employs high photon energies, such as 1486.6 eV for the Al K_α line, to investigate the electronic structure of the core levels. In contrast, ultraviolet photoemission spectroscopy (UPS) utilizes a lower energy of 21.22 eV, corresponding to the He I line, to study the valence electronic structure. Therefore, XPS and UPS can detect charge transfer and energy level alignment occurring at the heterointerface by observing the shifts in the core levels and Fermi energy levels, respectively (**Figure** 4a). All these techniques are critical prerequisites for forming robust heterojunctions and therefore determining the performance of AATs.

Most recently, operando photoemission electron microscopy (PEM) has been used to shed light on the detailed carrier-transport mechanism of anti-ambipolar α−6T/PTCDI-C8 heterojunctions (Figure 4b),[49] based on its capability to visually observe conductive electrons during the AATs operation.[52] When the AAT is turned on, PEM observations reveal the formation of a depletion layer at the lateral p-n junction, indicating the simultaneous pinch-off states of both p-type and n-type channels (Figure 4c).[49] The majority of electrons are observed to undergo recombination with the accumulated holes in the p-type semiconductor, resulting in an ≈80% reduction in photoemission intensity attributable to the recombination process.

Scanning probe microscopy has higher spatial resolution below 100 nm (i.e., the probe tip size) than the normal optical spectroscopy techniques. In 2019, the quantitative electrical imaging of WSe_2/MoS_2 anti-ambipolar heterojunctions was conducted by a scanning microwave impedance microscopy (MIM) (Figure 4d),[50] by which the lateral depletion region was clearly observed at the middle of the heterojunction (Figure 4e). The scanning MIM can detect and process the microwave reflection signal from the tip-sample interface, which allows us to directly measure the local variations in conductivity or permittivity of heterojunctions.[53]

Kelvin probe force microscopy (KPFM) was also employed to visualize the surface potential in organic α−6T/PTCDI-C8 heterojunctions (Figure 4f,g)[51] and the surface photovoltage map

Table 1. Characterization and analysis techniques for anti-ambipolar heterojunctions.

Technique	Mechanism	Related material properties	Spatial resolution
PL	Photo-excited luminescence	Bandgap, charge transfer	≈1 µm
Raman	Inelastic photon scattering	Vibrational modes	≈1 µm
XPS	Photoelectric effect	Core energy levels	≈10 µm
UPS	Photoelectric effect	Valence energy levels	≈10 µm
PEEM	Photoelectric effect	Spatial electron distribution	≈100 nm
MIM	Near-field microwave reflection	Electrical conductivity mapping	≈100 nm
KPFM	Electrostatic interaction	Surface potential distribution	≈10 nm
EFM	Electrostatic interaction	Surface potential distribution	≈10 nm

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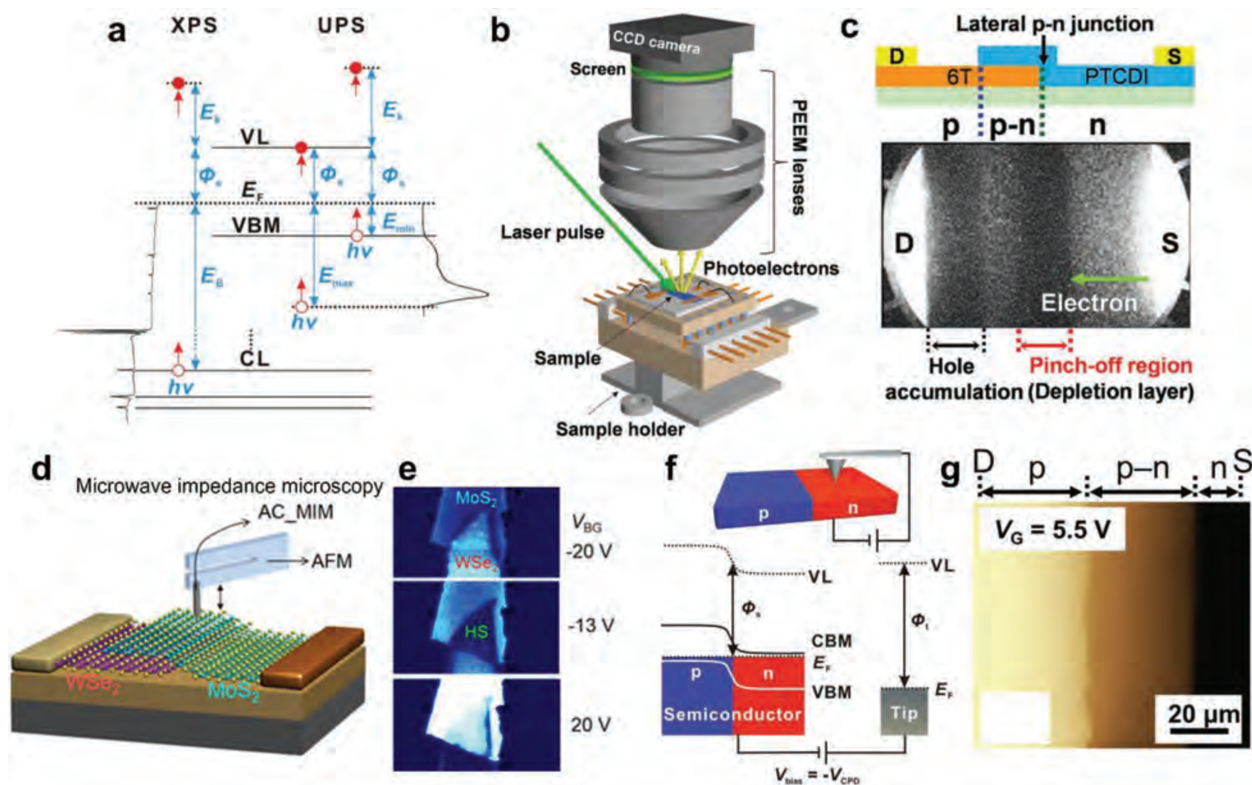

Figure 4. Characterization and analysis techniques. a) Schematic diagram of XPS and UPS spectra that define the relationships among the electron binding energy, the incident photon energy, the semiconductor work function, and the kinetic energy of emitted electrons.[48] b) PEEM measurement setup and c) PEEM imaging of 6T/PTCDI organic heterojunction measured at V_{peak}.[49] d) MIM measurement setup and e) MIM imaging of WSe_2/MoS_2 heterojunction.[50] f) KPFM measurement setup[48] and g) KPFM imaging of 6T/PTCDI organic heterojunction.[51] a, f) Reproduced with permission.[48] Copyright 2016, Wiley-VCH GmbH. b, c) Reproduced with permission.[49] Copyright 2022, Wiley-VCH. d, e) Reproduced with permission.[50] Copyright 2019, American Chemical Society. g) Reproduced with permission.[51] Copyright 2022, Wiley-VCH GmbH.

of $InSe/C_{70}$ heterojunctions.[47] The KPFM results provide direct evidence that the overlapped α−6T/PTCDI-C8 channel region function as a pseudo-drain electrode.[51] As a scanning probe microscopy technique similar to KPFM,[54] electrostatic force microscopy (EFM) was also used to perform surface potential mapping on anti-ambipolar heterojunction based on p-pentacene/n-MoS_2[55] and p-SnO/n-MoS_2.[56] Both KPFM and EFM operate based on the electrostatic interaction between the probe tip and the material surface. The major difference is that KPFM quantitatively measures the surface potential distribution, whereas EFM qualitatively measures the surface potential distribution through phase-shift detection in lift mode.

Overall, optical spectroscopy, photoemission spectroscopy, and scanning probe microscopy are valuable tools that enable a comprehensive understanding of the carrier transport mechanism in AATs. These techniques offer valuable insights that can contribute to enhancing device performance.[49,51]

3. Materials

Over the past few decades, the development of materials science has served as the primary catalyst for technological advancements in the semiconductor industry.[57–59] In pursuit of this objective, substantial efforts have been dedicated to preparing and applying new semiconductor nanomaterials, resulting in a substantial accumulation of experience in the field of anti-ambipolar heterojunctions.[9] Various semiconducting materials, including 2D, 1D, and bulk materials, have been employed to construct anti-ambipolar heterojunctions, as summarized in **Table 2**. Engineering the band structure of the two-component semiconductors is essential to enable efficient carrier transfer at the heterointerface. The material properties are primarily dictated by the variable structural and compositional characteristics, enabling the design and fabrication of materials with customized band structures that cater to specific device applications.[60–62] Moreover, in the case of low-dimensional nanomaterials, the quantum confinement effect and surface states play a key role in precisely adjusting the material properties and optimizing device performance.[37,63] In the following subsection, we will present an overview of the materials used in developing anti-ambipolar heterojunctions and their associated utilization principles.

3.1. 2D/2D Heterojunctions

The rise of 2D layered materials, known for their unique electrical, optical, and thermal properties, has sparked remarkable progress in fundamental scientific research and practical applications.[109–111] 2D materials have exhibited exceptional electrical properties and enhanced integration of devices with planar

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Table 2. Summary of the device performance of three-terminal AATs.

	AATs (p-/n-channels)	Dielectrics	V_{peak} [V]	I_{peak} [A]	ΔV_{ON} [V]	PVR	Methods	Notes	Refs.
2D/2D (Part 3.1)	BP/MoS_2	HfSiO	−1.8	3×10^{-6}	−2.5 to −1.5	$\approx 10^3$	ME/CVD	Large bandgap offset	[18]
	BP/MoS_2	SiO_2	0	4×10^{-6}	−3 to 3	–	ME/CVD	Self-alignment	[64]
	BP/MoS_2	HfO_x/SiO_2	–	–	−2.2 to 2	1.23	ME	hBN encapsulation	[65]
	BP/ReS_2	SiO_2	–	1×10^{-9}	–	–	ME	Type-III alignment	[66]
	BP/ReS_2	HfO_2	−2	2×10^{-5}	−4 to 0	10^3	ME	Type-III alignment	[67]
	$BP/MoTe_2$	SiO_2	−5	1×10^{-6}	−40 to 5	30	ME	–	[68]
	WSe_2/MoS_2	SiO_2	−42	3×10^{-10}	−53 to −30	$>10^3$	ME	–	[17]
	WSe_2/MoS_2	HfO_2	0.6	1×10^{-10}	0.4 to 0.8	≈ 10	ME	High-k dielectric	[17]
	WSe_2/MoS_2	SiO_2	−60	1×10^{-9}	−70 to −37	100	ME	Polymer acid treatment	[43]
	WSe_2/MoS_2	SiO_2	−5	–	−20 to 0	40	ME	–	[46]
	WSe_2/MoS_2	SiO_2	−10	1×10^{-9}	−15 to 0	$\approx 10^3$	ME	–	[50]
	WSe_2/ReS_2	SiO_2	−6.7	4×10^{-10}	−12 to −4	–	ME	Dual-gate	[69]
	WSe_2/SnS_2	SiO_2	−10	–	−20 to 0	>200	ME	–	[46]
	WSe_2/SnS_2	SiO_2	−5	1.5×10^{-7}	−15 to 5	10^5	ME	Light tunable	[70]
	WSe_2/SnS_2	hBN/SiO_2	5	3×10^{-8}	−9 to 17	10^4	ME	–	[71]
	WSe_2/InSe	hBN	−14	4×10^{-6}	−25 to −5	10^4	ME	Strain tunable	[72]
	WSe_2/graphene	SiO_2	10	5×10^{-7}	−15 to 20	>10	ME	–	[73]
	$MoTe_2/MoS_2$	SiO_2	−10	1×10^{-8}	−20 to 20	100	ME	Light tunable	[74]
	$MoTe_2/MoS_2$	SiO_2	−40	5×10^{-9}	−90 to −10	10^3	ME	Thickness modulation	[39]
	$MoTe_2/MoS_2$	hBN/SiO_2	0	1×10^{-6}	−50 to 50	10^5	ME	Photoinduced doping	[75]
	$MoTe_2/MoS_2$	hBN/SiO_2	−10	1×10^{-5}	−30 to 50	10^6	ME	RTA annealing	[76]
	$MoTe_2/Bi_2Se_3$	SiO_2	–	–	−23 to −5	–	ME	Topological insulator	[77]
	$MoTe_2$/InSe	SiO_2	−20	3.5×10^{-8}	−57 to 12	$>10^3$	ME	Photovoltaic effect	[78]
	$MoTe_2$/CrOCl	SiO_2	−20	3×10^{-8}	−40 to 0	–	ME	–	[79]
	TaS_2/MoS_2	SiO_2	0	–	−60 to 50	1.59	ME	T-junction	[80]
	$GeSe/SnS_2$	hBN	≈1	4.5×10^{-8}	−3 to 2	1.5×10^3	ME	Type-III alignment	[81]
Organic-Based (Part 3.2)	α−6T/PTCDI-C8	SiO_2	17	7×10^{-8}	0 to 30	5.9×10^4	Evaporation	First all-organic AATs	[33]
	α−6T/PTCDI-C8	Al_2O_3	0.25	1.6×10^{-7}	0 to 2.2	1.4×10^3	Evaporation	Interface engineering	[20]
	α−6T/PTCDI-C8	Al_2O_3	2.8	6×10^{-8}	2 to 5	$\approx 10^3$	Evaporation	Geometry engineering	[16]
	α−6T/PTCDI-C8	$Cytop/HfO_2$	−4.5	2×10^{-8}	−5.7 to −3.2	–	Evaporation	Dual-gate	[32]
	DNTT/PTCDI-C13	$Cytop/SiO_2$	−5	2×10^{-8}	−25 to 0	≈100	Evaporation	Light tunable	[82]
	DNTT/PTCDI-C13	pV3D3	5	1×10^{-7}	3.9 to 5.2	4.38	Evaporation	Asymmetric contact	[83]
	DNTT/PTCDI-C13	pV3D3	−1.5	5×10^{-8}	−2.6 to −0.8	12	Evaporation	3D stacking	[8]
	DNTT/PTCDI-C13	SiO_2	−15	5×10^{-8}	−25 to −10	10^3	Evaporation	–	[84]
	H-type/TTT-CN	air-gap	−18	1.5×10^{-7}	−31.5 to −7.5	1.6×10^3	Drop-casting	–	[42]
	DPA/CMUT	SiO_2	−35	4.5×10^{-6}	−50 to −20	–	Self-assembly	Light tunable	[45]
	C8-BTBT/PhC2-BQQDI	$PMMA/HfO_2$	−9	1.1×10^{-6}	−9 to −11	–	Evaporation	Mechanically flexible	[85]
	C8-BTBT/PTCDI-C8	$PMMA/HfO_2$	−6.6	2×10^{-7}	−8 to −5	–	Evaporation	–	[14]
	P(DPP2DT-T2)/P(NDI2OD-Se2)	PMMA: P(VDF-TrFE)	18	4.5×10^{-8}	10 to 25	1.3×10^4	Spin coating	–	[86]
	$Pentacene/MoS_2$	SiO_2	−30	1.5×10^{-7}	−60 to 20	10^3	Evaporation/ME	Photovoltaic effect	[55]
	$Pentacene/MoS_2$	SiO_2	−20	2×10^{-7}	−30 to 10	$>10^3$	Evaporation/ME	Trap-mediated transport	[87]
	$Pentacene/MoS_2$	SiO_2	−58	9×10^{-7}	−70 to −20	–	PVT/ME	Pentacene single crystal	[88]
	$CuPc/MoS_2$	SiO_2	−10	8×10^{-9}	−20 to 25	$\approx 10^4$	Evaporation/ME	–	[89]
	$Rubrene/MoS_2$	SiO_2	−4	4×10^{-8}	−20 to 5	4×10^3	PVT/ME	Rubrene nanosheet	[90]
	DNTT/ZnO	SiO_2	14	2×10^{-6}	0 to 30	10^6	Evaporation/ALD	Low power	[91]
1D-Based (Part 3.3)	$SWCNTs/MoS_2$	SiO_2	−2	1×10^{-8}	−20 to 20	$\approx 10^3$	Transfer/ME	First vdW AATs device	[21]
	$SWCNTs/MoS_2$	Al_2O_3	−1	1×10^{-6}	−4 to 2	100	Spin coating/CVD	Gaussian device	[92]
	SWCNTs/InGaZnO	HfO_2	2.2	2×10^{-6}	0.5 to 3.5	$>10^4$	Transfer/Spin coating	Wafer-scale uniformity	[93]

(*Continued*)

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Table 2. (Continued).

	AATs (p-/n-channels)	Dielectrics	V_{peak} [V]	I_{peak} [A]	ΔV_{ON} [V]	PVR	Methods	Notes	Refs.
	SWCNTs/In_2O_3	HfO_2	≈0	2×10^{-9}	0.16 to 0.6	>100	Inkjet printing	–	[94]
	SWCNTs/In_2O_3	HfO_2	1.3	5×10^{-7}	−1 to 2	21.55	Inkjet printing	–	[95]
	SWCNTs/In_2O_3	HfO_2	0.25	1×10^{-7}	0 to 0.6	–	Inkjet printing	–	[96]
	GaAsSb/InAs	HfZrO	0	1.9×10^{-8}	−0.3 to 0.3	50	MOVPE	Ferroelectric reconfigurable	[97]
	GaAsSb/MoS_2	SiO_2	−15	2.2×10^{-7}	−35 to 40	$\approx 10^3$	CVD/ME	AAT Phototransistors	[98]
	Te/Bi_2O_2Se	SiO_2	15	6×10^{-9}	10 to 30	$\approx 10^3$	CVD	Superlinear photocurrent	[19]
Homojunctions (Part 3.4)	Graphene	AlO_x/HfO_2	1	6×10^{-5}	−2 to 4	–	ME	Electrostatic control	[99]
	Graphene	SiO_2		–	0 to 18	–	CVD	Charge transfer doping	[100]
	Graphene	SiO_2	0	1×10^{-4}	−36 to 31	–	CVD	Optical gating	[101]
	MoS_2	SiO_2	−10	4×10^{-7}	−20 to 10	47	ME	Doped by substrate	[102]
	WSe_2	hBN	−2.1	1×10^{-8}	−3 to −0.8	≈10	ME	Stepped dielectric	[103]
	WSe_2	hBN/SiO_2	5	2×10^{-11}	−5 to 15	>10	ME	Thickness-induced band offset	[104]
	WSe_2	SiO_2	−6	8×10^{-10}	−21 to 6	40	ME	Light tunable contact	[105]
	WSe_2	hBN	0	1×10^{-8}	−1 to 1	>100	ME	Electrostatic control	[106]
	WSe_2	hBN	−5	1×10^{-10}	−6 to −4	10	ME	Electron-beam treatment	[107]
	$MoTe_2$	hBN/SiO_2	0	1×10^{-8}	−35 to 30	≈50	ME	hBN engineering	[108]

Abbreviations: ME, mechanical exfoliation; CVD, chemical vapor deposition; PVT, physical vapor transport; MOVPE, metal–organic vapor-phase epitaxy.

wafer technologies.[112–114] Furthermore, a wide range of electrical and chemical properties exhibited by 2D materials has provided enormous flexibility in material selection and band alignment design, thereby expediting the progress of innovative devices.[7,115–117] Heterojunctions formed from conventional bulk materials often encounter limitations arising from lattice mismatches, surface imperfections, and dangling bonds. Differently, 2D/2D heterojunctions are created by stacking layered materials using weak vdW interactions, eliminating lattice mismatches or interfacial defects. The interfaces in vdW heterostructures are sharper than those in traditional crystalline Si, Si-Ge, and III-V semiconductor heterojunctions, resulting in superior quality. The quality of the heterojunction is of great importance in ensuring the reliability of band-to-band tunneling behaviors, which are responsible for the nonlinearity observed in electrical characteristics.[118] By manipulating the band alignment at heterojunctions, which can be achieved through type-I (straddling gap), type-II (staggered gap), and type-III (broken gap) alignments, there is a promising potential to optimize the performance of 2D/2D anti-ambipolar heterojunctions.[119,120]

3.1.1. TMDCs-Based Heterojunctions

Transition metal dichalcogenides (TMDCs) have attracted substantial scientific interest recently. Representative cases such as MoS_2 and WSe_2, belonging to the TMDCs family, exhibit stable chemical structures, rendering them highly promising for constructing dependable, defect-free, and atomically sharp heterointerfaces.

In 2015, the demonstration of band-to-band tunneling in vertical p-WSe_2/n-MoS_2 van der Waals (vdW) heterojunctions highlighted the presence of an atomically sharp interface with minimal trap states (**Figure 5a**).[121] By employing a symmetric dual-gate device architecture, the gate tunable vdW heterojunctions have the ability to operate as either an NDR Esaki diode, a backward tunneling diode, or a forward rectifying diode by adjusting the applied gate bias. Due to the weak electrostatic screening by the ultrathin 2D materials, a substantial gate coupling efficiency of ≈80% is achieved, enabling the modification of interlayer band alignments and electron tunneling. As shown in Figure 5b, the NDR peak position and PVR are governed by the applied gate voltages. The demonstrated interlayer coupling and electron tunneling in 2D heterojunctions show the possibility of building 2D layered tunnel transistors for low-power electronics. However, the band-to-band tunneling of the above-mentioned dual-gated MoS_2/WSe_2 diode emerged at a cryogenic temperature of 77 K.

In 2015, p-WSe_2/n-WS_2 vdW heterojunction transistors were also built by Li et al. to show distinct rectifying, ambipolar, and anti-bipolar characteristics at room temperature (Figure 5c).[122] Rectifying properties characterized by a forward-to-reverse current ratio of 10^2, as well as ambipolar behaviors with a PVR of 10^3, were demonstrated in this work. Figure 5d shows three regions in the heterojunction transistors with varying positive drain voltage. During the device operation, the electrical transport follows three successive stages as V_{ds} increases: in stage-I, anti-ambipolar behavior is observed, which is controlled by the combined operation of diffusion current and junction effect; in stage-II, p-type behavior predominates, primarily influenced by the p-type WSe_2 channel; and in stage-III, ambipolar behavior arises from the collective operation of the p-type WSe_2 channel and n-type WS_2 channel. The type-II band alignment of this p-n vdW heterojunction enables efficient separation of electrons and holes, thereby inducing a prominent photovoltaic effect with self-driven photoresponse.

In 2016, with an electron affinity difference of 0.4 eV, the p-WSe_2/n-MoS_2 heterojunction was constructed to display band-to-band tunneling (with a curvature coefficient of 62 V^{-1}) and

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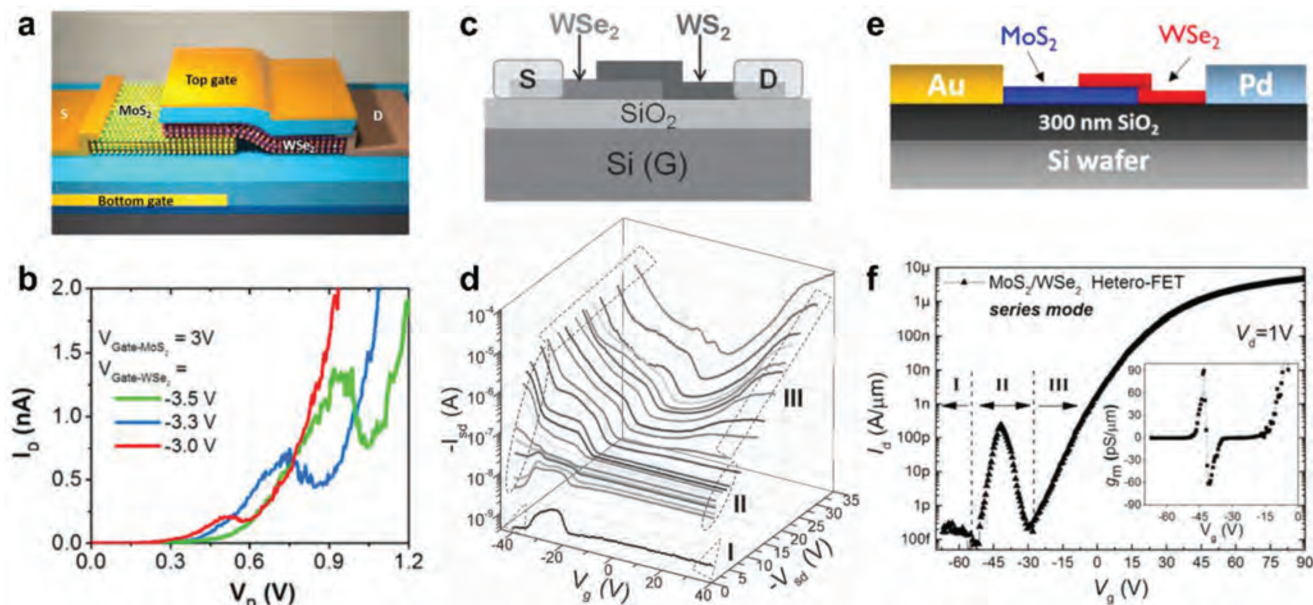

Figure 5. TMDCs-based heterojunctions. a) 3D schematic illustration and b) gate-controlled NDR behavior of the p-WSe_2/n-MoS_2 vdW heterojunction device.[121] c) Device structure and d) transfer characteristics of the vertically stacked WSe_2/WS_2 heterojunction transistors with different drain voltage.[122] e) Device structure and f) transfer characteristics p-WSe_2/n-MoS_2 heterojunction AATs.[17] a, b) Reproduced with permission.[121] Copyright 2015, American Chemical Society. c, d) Reproduced with permission.[122] Copyright 2015, Wiley-VCH. Reproduced with permission.[17] Copyright 2016, American Chemical Society.

positive-to-negative transconductance transition (with a PVR more than 10^3 shown in Figure 5e,f).[17] The transition in transconductance at room temperature is attributed to the effective modulation of the charge density and energy band of the 2D layers, primarily induced by the strong interlayer coupling. This work also confirms that band-to-band tunneling predominantly occurs in the in-plane direction of the overlapped region, as evidenced by the smaller effective heterojunction bandgap at the lateral edge compared to the out-of-plane direction. At this early stage, the anti-ambipolar behaviors of 2D heterojunctions are still far from ideal characteristics; more device optimization routes will be discussed in later sections.

3.1.2. BP-Based Heterojunctions

The strong interlayer coupling at the interface enables the 2D layered materials to generate a significant bandgap offset, resulting in a high on-off ratio and favorable rectifying characteristics.[123] For instance, a well-designed p-BP/n-MoS_2 heterojunction has an electron affinity difference of only 0.1 eV between two materials (**Figure 6**a),[18,124] by which energy band offset can easily be tuned. The energy band structure of p-BP/n-MoS_2 heterojunction under different biases can be found in Figure 6b, as reported by Wu et al. in 2017. With the sweeping of V_G from negative to positive, transfer curves of the lateral p-BP/n-MoS_2 transistor changed from n-MoS_2 dominating channel to p-BP dominating channel (Figure 6c).

In 2018, more pronounced and tunable anti-ambipolar Λ-shaped transfer characteristics were witnessed in p-BP/n-MoS_2 heterojunction enabled by a self-aligned, semi-vertical, and source-gated architecture (Figure 6d),[64] which is also reproduced by finite-element device simulations. As shown in Figure 6e, the resulting anti-ambipolar Gaussian characteristics with large PVR and nearly complete tunability bring a unique ability for signal processing applications, such as frequency-shift keying and phase-shift keying. It should be noted that the unique geometry offers enhanced electrostatic control and high current density in short-channel devices. However, particular attention should be given to minimizing the parasitic capacitance, particularly in high-frequency application circuits.

3.1.3. 2D Heterojunctions with Type-III Alignment

Using type-III broken-gap band alignment, NDR devices have been fabricated based on 2D phosphorene/rhenium disulfide (BP/ReS_2) heterojunctions.[66,125,126] In 2016, to elucidate the operations of such an NDR device, the tunneling/diffusion currents and parasitic resistance were examined at different temperatures.[125] As a result, the PVR values of 4.2 (at room temperature) and 6.9 (at 180 K) were obtained. The authors proposed that, in comparison to a type-II band alignment, a type-III broken-gap band alignment enables the facile formation of a highly doped P^+/N^+ heterojunction, typically achieved through electrostatic doping or chemical doping processes. In general, no energy band overlap near broken-gap heterojunctions could bring diverse current-transport characteristics in a single device.

In 2019, with the evolution of BP thickness increasing from 5 to 100 nm, the BP/ReS_2 heterojunction device with different band-bending conditions could function as gate tunable

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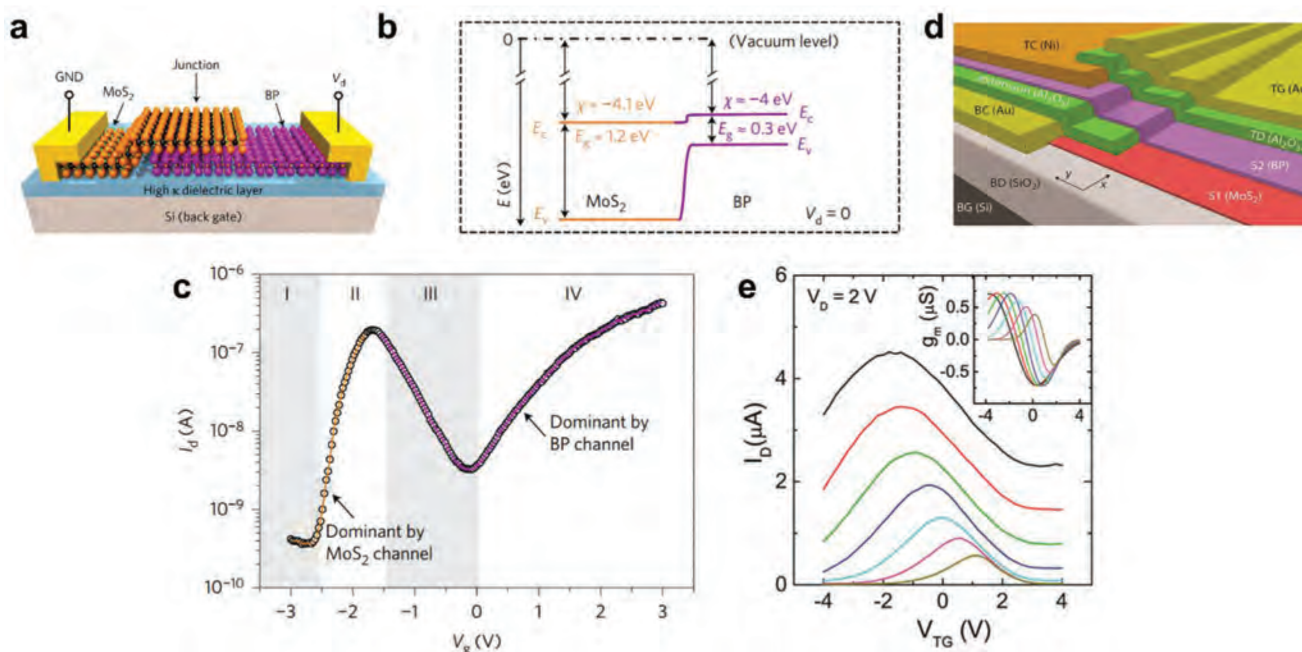

Figure 6. BP-based heterojunctions. a) Schematic view, b) energy band diagrams, and c) transfer curves of the lateral p-BP/n-MoS_2 heterojunction transistor.[18] d) Schematic view and e) anti-ambipolar transfer characteristic curves of self-aligned p-BP/n-MoS_2 heterojunction transistors.[64] Inset of e) shows the corresponding variation in transconductance. a–c) Reproduced with permission.[18] Copyright 2017, Springer Nature. d,e) Reproduced with permission.[64] Copyright 2018, American Chemical Society.

P-N junctions, Esaki diodes, backward-rectifying diodes, and non-rectifying devices.[66] This multifunctional device may boost the development of compact circuits with a significantly reduced need for multiple semiconducting materials or junctions.

Tao et al. designed a type-III broken-gap tunneling heterojunction based on ambipolar 2H-$MoTe_2$ and n-doped Bi_2Se_3.[77] In this study, the transport property of $MoTe_2$/Bi_2Se_3 heterojunctions is determined by the thermionic emission and tunneling process of the majority carrier, which refers to electrons. This finding contrasts the conventional type-II p-n junction based on the diffusion process of minority carriers. Notably, this work may be the first to use topological insulators (such as Bi_2Se_3 or Bi_2Te_3) to construct a vdW tunneling heterojunction. Interestingly, based on first-principles calculations, a transition from type-III to type-II band alignment was realized in intrinsic type-III ZrS_2/WTe_2 vdW heterojunction by applying an external electric field and strain effect.[127]

3.1.4. Device Optimization of 2D Heterojunction

An optimized device geometry would be useful for achieving suitable driving on-state voltage range and high PVR in AATs. Thus far, various strategies supported by systematic experiments and theories have been employed in 2D heterojunction AATs, e.g., selecting suitable p- or n-type 2D component channels, appropriate channel thickness, a suitable insulating layer, etc. Using a series of improving strategies mentioned above, a modified SnS_2/WSe_2 heterojunction-based AAT was successfully fabricated with a more apparent Λ-shaped transfer curve, a steeper drain-source current, and a PVR of 200.[46] When two-layer MoS_2 (bandgap ≈1.37 eV) and few-layer $MoTe_2$ (bandgap ≈0.94 eV) were utilized in a 2D heterojunction, strong NDT behavior with a large PVR of ≈10^3 was observed, enabled by a rational design of the layer thickness-dependent band structures.[39] With a large vdW barrier and improved interface recombination, p-WSe_2/n-SnS_2 or p-WSe_2/n-MoS_2 heterojunction AATs exhibited a high PVR exceeding 10^4 at room temperature, while the ternary inverter built on them show a broad middle logic plateau with a width of 45 V.[71]

Kim et al. used a surface modification strategy to gain the distinguishable AAT behavior in WSe_2/MoS_2 heterojunction transistors for achieving stable ternary inverter characteristics.[43] In this work, a surface treatment was conducted using poly(methyl methacrylate-co-methacrylic acid) that features electron-rich carboxyl acid moieties. Through a surface-electronic transfer process, the charge density of the WSe_2 and MoS_2 layers could be adjusted to an optimized level.

Additionally, a photoinduced doping treatment was employed to adjust the $MoTe_2$ and MoS_2 layers to their optimal conditions, enabling the formation of an anti-ambipolar device (**Figure** 7a,b).[75] To conduct photoinduced doping, UV illumination, and large writing gate voltage were applied simultaneously on the samples with a typical treatment duration of 1s. Given the highly effective and nonvolatile band modulation, together with comparable doping levels in the p- and n-channels, $MoTe_2$/MoS_2 heterojunction-based AATs demonstrate a PVR of ≈10^5, an on-state current at the μA level and the ability to tune the V_{peak} position (Figure 7c).[75]

The anti-ambipolar behavior of the $MoTe_2$/MoS_2 heterojunction was further enhanced, achieving a PVR of ≈10^6 through a rapid thermal annealing (RTA) process in a hydrogen mixture

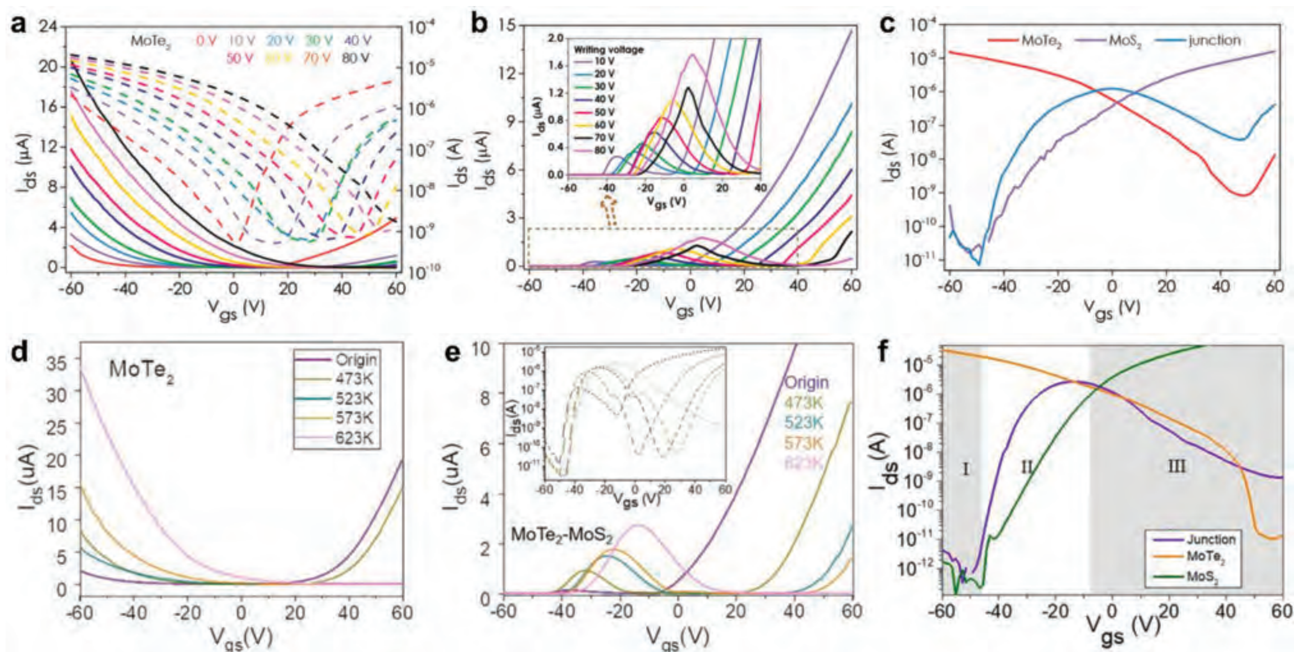

Figure 7. Device optimization of 2D/2D heterojunctions. Transfer curves of a) $MoTe_2$ and b) $MoTe_2/MoS_2$ heterojunction after photoinduced doping treatment with different writing voltages.[75] c) Transfer curves of $MoTe_2$, MoS_2, and $MoTe_2/MoS_2$ heterojunction after photoinduced doping with a writing voltage of 80 V.[75] Transfer curves of d) $MoTe_2$ and e) $MoTe_2/MoS_2$ heterojunction after the RTA process with different treatment temperatures.[76] f) Transfer curves of $MoTe_2$, MoS_2, and $MoTe_2/MoS_2$ heterojunction after 623 K RTA treatment.[76] a–c) Reproduced with permission.[75] Copyright 2019, American Chemical Society. d-f) Reproduced with permission.[76] Copyright 2019, AIP Publishing.

atmosphere (Figure 7d–f).[76] This effect is ascribed to producing p-type defects at the metal/$MoTe_2$ interface through RTA, generating a substantial overlap in the on region between the p-type $MoTe_2$ and the n-type MoS_2 channels. The resulting PVR value of 10^6 is one of the highest reported at that time, surpassing previous works by several orders of magnitude. The dynamic and precise modulation of transport properties in AATs has great potential to inspire the development of advanced functional devices.

The quality of the vdW heterointerfaces plays a critical role in achieving high-performance 2D NDR/NDT devices, particularly for air-unstable layered materials such as BP and $SnSe_2$. To fulfill this aim, in 2019, a $SnSe_2/WSe_2$ heterojunction was constructed in inert gas environments.[128] This approach efficiently suppresses the oxidation layers forming at the heterointerfaces and produces a clean channel for band-to-band tunneling.[118] Notably, black phosphorus is unstable in ambient and may rapidly degrade in a short exposure period.[129] In the work by Wu et al., benefiting from the h-BN encapsulation, gate-tunable BP/MoS_2 heterojunction shows the stable and continuous transition of NDR behavior, revealing application potentials in multifunctional electronics.[65]

In 2019, Cheng et al. reported the dynamic tunability of anti-ambipolar transport in a 2D heterostructure device, where the $MoTe_2$ channel is integrated with a graphene/h-BN floating gate.[130] Employing a unique asymmetric semi floating-gate structure, the $MoTe_2$ channel is positioned vertically above the floating gate in one half, while the other half does not have this configuration. The resulting asymmetric electrical field influences the recombination and diffusion currents, which in turn controls the V_{peak} and NDT feature, enabling a peak current modulation of $\approx 5 \times 10^3$.

3.2. Organic-Based Heterojunctions

Compared to 2D materials usually fabricated by a mechanical exfoliation method, organic materials, and their heterojunctions provide advantages regarding synthetic tunability, solution processability, and deposition scalability.[131–134] In 1995, the ambipolar characteristics were discovered in organic heterostructure transistors, explicitly utilizing a vertical p-type 6T/n-type C_{60} molecular junction.[135] This breakthrough significantly advanced the development of organic light-emitting transistors and other organic heterojunction devices.[136,137] Subsequently, with the advancement of the deposition technique and photolithography process, the lateral organic p-n heterostructures are explored to endow more powerful devices.[138,139] As an example, the organic anti-ambipolar heterojunction architecture entails stacking p-type and n-type organic semiconductors, creating a partially overlapped channel region. When subjected to gate bias, this produces an imbalance in the charge transport properties, resulting in negative-transconductance electrical behaviors recently gaining substantial interest.[34,35,140]

3.2.1. All-Organic Heterojunctions

An all-organic heterojunction transistor with p-type α-sexithiophene (α−6T) combining n-type N,N'-dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C8) as the channel was built

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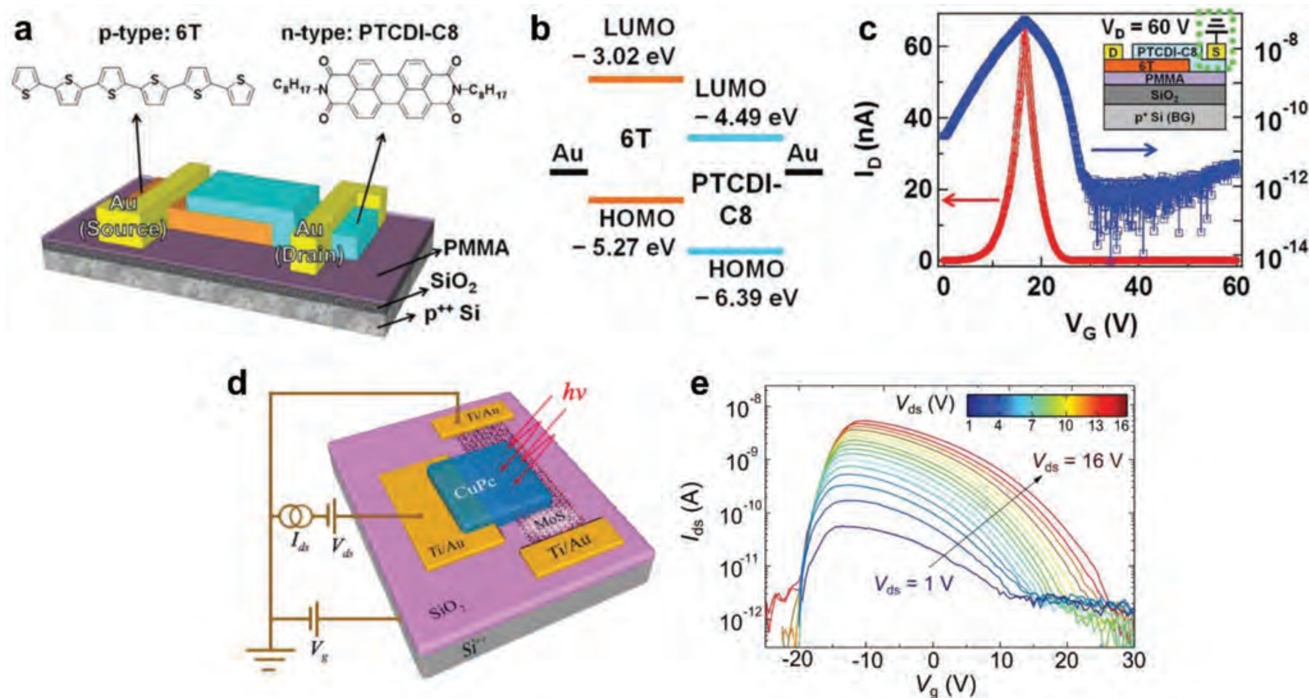

Figure 8. Organic-based heterojunctions. a) Schematic illustration, b) energy level alignment, and c) transfer curves of organic p-type 6T/n-type PTCDI-C8 heterojunction AATs.[33] d) Device illustration and e) transfer characteristics of Cu-phthalocyanine/MoS_2 hybrid organic–inorganic heterojunctions. a–c) Reproduced with permission.[33] Copyright 2017, Wiley-VCH. d,e) Reproduced with permission.[89] Copyright 2015, Royal Society of Chemistry.

in 2017 (**Figure** 8a).[16,33] The type-II energy band alignment, combined with comparable carrier mobilities in the two organic semiconducting materials, further facilitates the balanced transport of electrons and holes (Figure 8b). As a result, the device demonstrated room-temperature anti-ambipolar behavior, including a PVR of 10^2 for antihole operation and 10^4 for antielectron operation (Figure 8c).[33] By modifying the thickness of the α−6T channel, the PVR, V_{peak}, and g_m values of the heterojunction transistor could be adjusted to realize simple ternary inverter functions.[20]

By implementing device refinements such as local gating and dielectric engineering,[108] it is possible to narrow the on-state voltage window,[141] leading to improved operating frequency, reduced energy consumption, and increased switching gains in MVL devices. To control the device properties of organic p-type 6T/n-type PTCDI-C8 heterojunction AATs, interface engineering was explored on the channel/electrode interfaces and channel/dielectric interface, in order to improve the carrier injection and carrier accumulation, respectively.[20] The suitable selection of carrier injection interlayers (Mo_2O_3 or Cs_2CO_3) and a high-κ insulator layer (Al_2O_3) could enable a low V_{peak} of 0.25 V, a narrow ΔV_{ON} of 2.2 V, and a PVR of 10^4.

The previously mentioned devices were primarily produced using vacuum deposition techniques. Actually, organic electronics are widely recognized for their solution (or printing) processability. However, all-organic AATs produced through solution processing remain unreported. In recent studies, the constituent materials of organic electronics, including the p- and n-channels, the dielectric layer, and electrodes, have all been composed of polymeric materials.[86] This indicates that, like other organic electronic devices, organic MVL circuits can potentially be fabricated through a solution process. The challenge of achieving solution processability in AATs and MVL circuits can be attributed to the difficulty of forming a pn-heterojunction. Stacking soluble organic semiconductors with sharp and flat heterojunctions is challenging due to their miscibility. To achieve compatible processability in organic AATs, it is vital to carefully select organic semiconductors that can be dissolved in specific solvents.

For a kind of disordered semiconductor material, achieving precise control over film fabrication and alignment of the organic heterojunction is of utmost importance. Considering this, the flatness and molecular orientation at the heterointerface should be well designed. To this end, in 2018, self-assembled single-crystalline organic monolayers were produced by a general bottom-up two-dimensional spatial confinement method.[45] Using this method, lateral organic monolayer p-n junctions based on p-type 2,6-diphenylanthracene (DPA) and n-type dicyanomethylene-substituted fused tetrathienoquinoid (CMUT) were built by a mechanical transfer process. The laterally connected p-n junction, characterized by excellent device performance uniformity, plays a significant role in achieving a distinct anti-ambipolar switching behavior.

3.2.2. Organic–Inorganic Hybrid Heterojunctions

The surface atoms of small molecular and polymeric organics possess saturated bonds, thus endowing them with vdW interactions for integration with other dangling bond-free vdW materials, e.g., 2D layered materials.[47,142–144] From

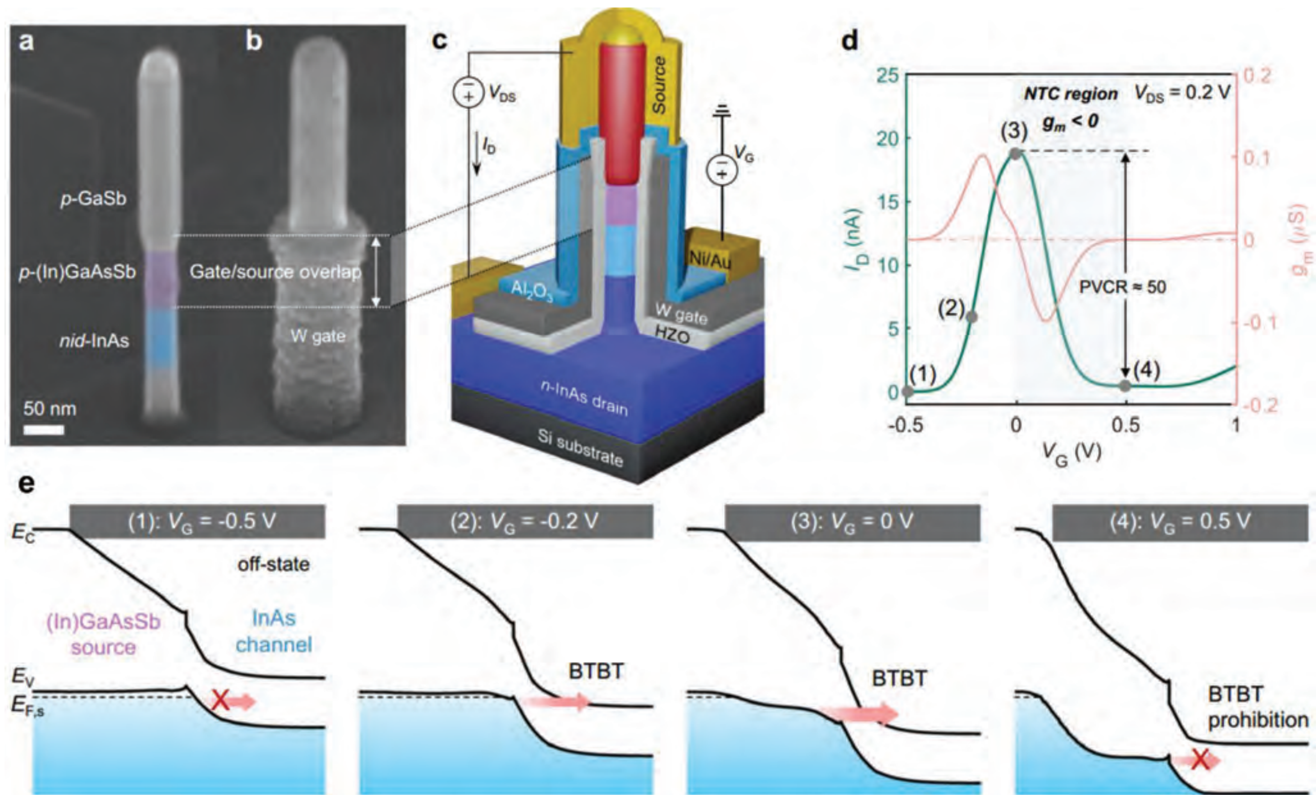

Figure 9. Vertical nanowire heterojunctions. a) SEM images and b) corresponding vertical gate-all-around tunnel III-V nanowire ferroelectric AATs. c) Schematic illustration, d) anti-ambipolar NDT behaviors, and e) schematic band diagrams under different gate voltages of vertical nanowire ferroelectric AATs.[97] a–e) Reproduced with permission.[97] Copyright 2023, Springer Nature.

2015, hybrid p-n heterojunctions of pentacene/MoS_2,[55,87,88] Cu-phthalocyanine/MoS_2 (Figure 8d,e),[89] and Rubrene/MoS_2[90] were built to demonstrate gate-tunable anti-ambipolar transfer characteristic. The organic-2D hybrid heterojunctions exhibit favorable gate-controlled photoresponse facilitated by photogating and photovoltaic effects. In this process, photoinduced carriers are predominantly generated in the organic layer, while the role of the 2D materials primarily lies in controlling charge separation.[89]

Kim et al. proposed that the rich charge trap states in organic semiconductors, usually with a density on the order of $\approx 10^{18}/cm^3$, could mediate the electronic transport properties of pentacene/MoS_2 heterojunction AATs.[87] Dong et al. reported that high-quality pentacene single crystals could give pentacene/MoS_2 organic–inorganic vdW heterojunctions with higher output current density and clear anti-ambipolar switching characteristics compared to polycrystalline pentacene films.[88] Overall, the organic molecular and polymer semiconductors are free of dangling bonds, suggesting new opportunities for vdW heterostructures.

In 2022, Lee et al. reported the anti-ambipolar operation of p-DNTT/n-ZnO hybrid heterojunctions with a high PVR $\approx 10^6$ and good operating reliability.[91] The complete device fabrication process was carried out using a low thermal budget below 200 °C, making it compatible with back-on-the-line or monolithic 3D integration. Furthermore, ternary full adder circuits utilizing p-DNTT/n-ZnO hybrid AATs were successfully demonstrated, exhibiting a remarkable low power operation capability of ≈0.15 μW.[145] This power consumption is significantly lower compared to other device candidates.

3.3. 1D-Based Heterojunctions

The continuous trend of device miniaturization is critical in advancing modern semiconductor electronics. Among various material systems, 1D materials have demonstrated numerous advantages, including superior carrier transport, energy efficiency, flexibility, and scalability, often surpassing their counterparts.[57,62,146]

3.3.1. Vertical Nanowire Heterojunctions

In 2023, vertical gate-all-around tunnel nanowire FETs were built with a ferroelectric Zr-doped HfO_2 (HZO) insulting layer wrapping on an III-V nanowire (**Figure** 9a–c).[97,147] The vertical nanowire device exhibited a remarkable reduction in device footprint (≈0.01 μm²) and supply voltage (as low as 50 mV).[148] With proper doping concentrations, the n-doped InAs/intrinsic InAs/p-doped (In)GaAsSb junction showed NDT behaviors (Figure 9d), while the carrier transport is dominated by the band-to-band tunneling process (Figure 9e). More importantly, the presence of ferroelectricity in the HZO insulating layer allows

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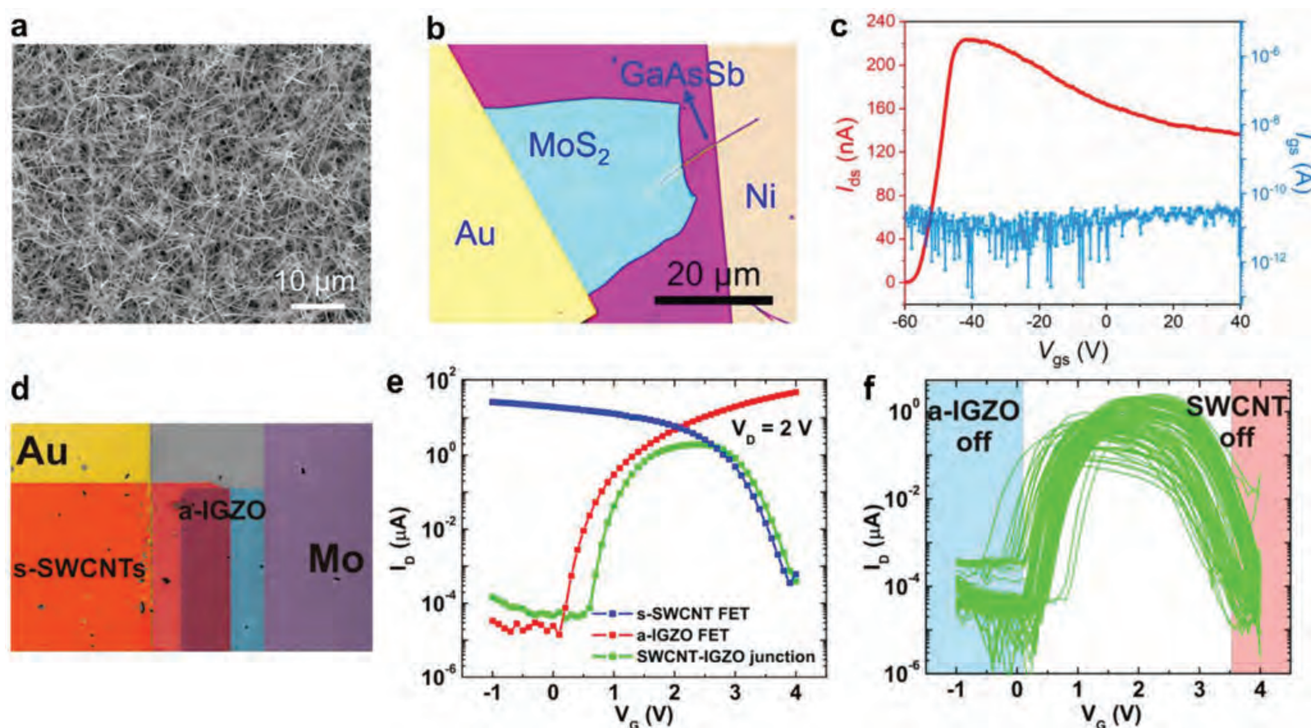

Figure 10. Mixed-dimensional 1D/2D heterojunctions. a) SEM image of VLS-grown GaAsSb nanowires. b) Optical image and c) transfer characteristics of anti-ambipolar 1D GaAsSb/2D MoS_2 heterojunction device.[98] d) Optical image and c) transfer characteristics of anti-ambipolar SWCNTs/a-IGZO heterojunction device. Anti-ambipolar switching of 115 separate SWCNTs/a-IGZO heterojunction devices.[93] a–c) Reproduced with permission.[98] Copyright 2022, American Chemical Society. d–f) Reproduced with permission.[93] Copyright 2015, American Chemical Society.

for reconfigurable NDT behaviors in the vertical nanowire ferroelectric FETs, including a PVR $\approx 10^2$ and a high symmetry AATs transfer curve.[97,149] After that, signal modulation circuits were also constructed based on reconfigurable vertical nanowire AATs to demonstrate different frequency multiplication, shifting, and mixing functions. This study showcases the potential of integrating high-density vertical nanowire AATs into energy-efficient, multifunctional digital/analog hybrid circuits.

3.3.2. Mixed-Dimensional 1D/2D Heterojunctions

The mixed-dimensional heterostructures of 1D/2D materials exhibit notable advantages, such as the optimized resistance-capacitance time constant.[150–153] For instance, the forward research in mixed-dimensional 1D/2D anti-ambipolar heterojunctions has revealed superior (opto-)electronic properties, including 1D GaAsSb/2D MoS_2 heterojunction and 1D Te/2D Bi_2O_2Se heterodiode.[19,98] Furthermore, mixed-dimensional 1D/2D heterojunctions enable us to explore unique physical properties that differ from conventional bulk junctions, e.g., the efficient interlayer coupling and ultrafast charge transfer in 1D WO_{3-x}/2D WSe_2 heterostructure reported lately.[154]

The formation of type-II band alignment, together with the strong interfacial coupling in the 1D GaAsSb/2D MoS_2 heterojunction, enabled the exploration of anti-ambipolar switching behaviors (**Figure** 10a–c).[98] The same work introduces the resistance-capacitance time constant to rationally design the nanoscale photosensitive channel. Unlike organic-based or 2D/2D heterojunctions, ultrathin 1D/2D devices with reduced active areas exhibit an optimized resistance-capacitance time constant. This inherent characteristic enhances the response speed and switching gains, as observed in the 1D Te/2D Bi_2O_2Se heterodiode.[19] In 2020, single SWCNT combined with multilayer WSe_2 was utilized to construct 1D/2D mixed-dimensional atomic heterojunction,[155] featuring an ultimate-scaled nanometer functional area and pronounced band-to-band tunneling and thermal emission phenomena.

3.3.3. CNTs-Based Heterojunctions

Carbon nanotubes (CNTs) share similarities with 2D materials, as they are defect-free and possess a vdW surface. In 2013, Jariwala et al. exploited the solution processability of SWCNTs to establish a vdW heterointerface with monolayer MoS_2, by which stable ambient operation and a PVR of up to 10^4 were obtained.[21] This SWCNTs/MoS_2 anti-ambipolar heterojunction could also work as a photodiode, exhibiting an external quantum efficiency of 25% and a rapid photoresponse below 15 μs.

Following that, to achieve sufficient scalability and/or homogeneity for large-area integrated circuits, the same group reported the p-n heterojunctions based on p-type SWCNTs and n-type amorphous indium gallium zinc oxide (a-IGZO) thin films (Figure 10d).[93] It should be noted that both SWCNTs and a-IGZO films can be processed using solution methods,

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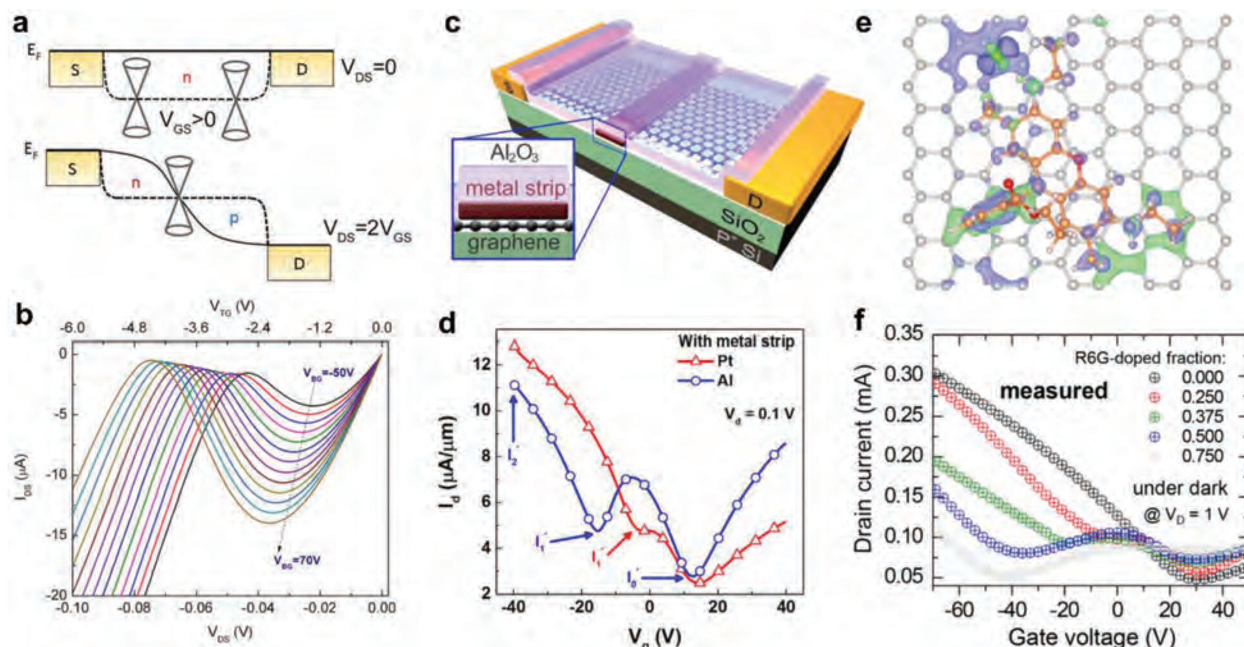

Figure 11. Graphene homojunctions. a) Band diagrams of graphene channel under different drain biases.[157] b) Tunable NDR behaviors in graphene dual-gated FET.[99] c) Device illustration and d) transfer characteristics of graphene FET decorated with different metal strips.[100] e) The electron density difference at the interface between graphene and R6G. f) Transfer curves of graphene p-n junction transistors with different R6G-doped areas.[101] a) Reproduced with permission.[157] Copyright 2012, American Chemical Society. b) Reproduced with permission.[99] Copyright 2013, AIP Publishing. c,d) Reproduced with permission.[100] Copyright 2016, Springer Nature. e,f) Reproduced with permission.[101] Copyright 2018, American Chemical Society.

possessing high spatial uniformity and good stability in ambient conditions. A sequence of well-established manufacturing methods, including standard photolithography, etching technique, and high-κ gate dielectrics utilization, work together to provide low-voltage anti-ambipolar operation, a PVR above 10^4 (Figure 10e), and good device uniformity at the wafer scale (Figure 10f).[93]

Enabled by the solution processability, in 2019, an inkjet printing method was employed by Kim et al. to build gate-tunable anti-ambipolar heterojunctions consisting of dissimilar p-type SWCNTs and n-type metal oxides (e.g., In_2O_3) thin films.[94,95,156] Inkjet printing, a scalable and cost-effective method for device fabrication, has demonstrated considerable potential in producing low-cost electronic devices by eliminating the need for complex photolithography steps. Plasma treatment is essential to modify the surface conditions for forming continuous films, by which the partially overlapped SWCNTs/In_2O_3 heterojunction region is obtained.[94] Drop-on-demand inkjet printing enables the selective deposition of semiconductor inks onto the desired area with controlled morphology, allowing to regulate the performance of SWCNTs/In_2O_3 AATs (e.g., I_{peak}, V_{peak}, and PVR) as well as ternary inverter circuits (e.g., balance logic states and gain).[156]

3.4. Homojunctions

A homojunction refers to a semiconductor interface formed between layers of the same semiconducting materials. In a homojunction, the materials have equal band gaps but often differ in terms of doping levels. Compared to the heterojunction made by dissimilar materials, the anti-ambipolar homojunction study of the same component materials is lacking, though it is structurally simple and easy to integrate. To achieve homojunction, external fields, such as electric field, light field, and strain, are usually needed to induce the imbalance of carrier distribution.

3.4.1. Graphene Homojunctions

Graphene has the potential to exhibit nonlinear electrical behavior due to its unique Dirac-cone band structure.[158] Despite the gapless and symmetric band structure of graphene, the Fermi level can be modified above or below the Dirac point through direct charge-carrier doping. This can result in the shift of the minimum conductivity voltage and even the complete inversion of the charge carrier type in a graphene transistor (**Figure 11a**).[157,159] In a three-terminal graphene transistor architecture, it is possible to establish a homojunction within the channel region by applying suitable electrical potential through the gate or drain electrodes.[157] The utilization of three-terminal graphene NDR devices provides greater operational flexibility, offering an alternative avenue for graphene applications.

Following that, utilizing these NDR characteristics, Liu et al. exhibited the potential for implementing non-Boolean logic circuits based on graphene dual-gated FET (Figure 11b).[99] By precisely modifying the applied gate and drain voltages, various logic functions were achieved, including NOT, NAND, and XOR gates. In the same paper, first-principles atomistic modeling revealed that the NDR effect was observed in both the

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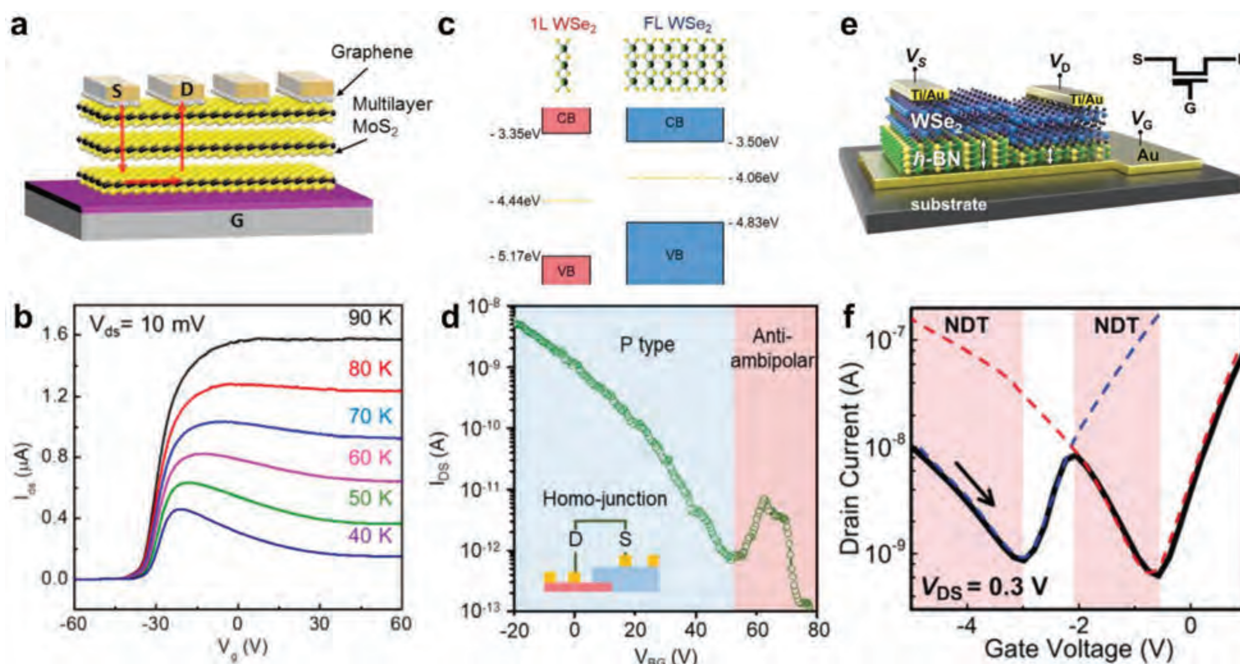

Figure 12. TMDCs homojunctions. a) Device illustration and b) transfer characteristics of the multilayer MoS_2 transistor with different measured temperatures.[102] c) Energy band structures of monolayer and few-layer WSe_2. d) Transfer characteristics of homojunction based on monolayer and few-layer WSe_2.[104] e) Device illustration and f) transfer characteristics of WSe_2 transistors with stepped h-BN dielectric.[103] a,b) Reproduced with permission.[102] Copyright 2017, American Chemical Society. c,d) Reproduced with permission.[104] Copyright 2022, Wiley-VCH. e,f) Reproduced with permission.[103] Copyright 2020, Royal Society of Chemistry.

drift-diffusion and ballistic regimes, suggesting their potential application in downscaled electronics. The systematic simulations demonstrate that the primary mechanism underlying the NDR behavior in dual-gate graphene FETs is associated with the interplay between carrier density and drift velocity.[158] Similar operation mechanisms also serve as the basis of ambipolar multilayer BP transistors,[25] where the NDR effect is influenced by the electrical field-dependent carrier density modulation and carrier-type switching.

In a more practical strategy, a metal strip of Al or Pt was deposited on the middle of the graphene channel to create a p-n-p or n-p-n staggered homojunction (Figure 11c,d).[100] The effectiveness of this approach highly depends on the work function of the metal strip. The temperature-dependent hydrogen interface diffusion was proposed to affect the charge transfer process and thus regulate the anti-ambipolar features. Applying a similar spatial surface doping concept, researchers utilized an organic dye, rhodamine 6G (R6G), to manipulate the NDT behaviors of graphene, such as the V_{peak}, output current level, and fold-back structure (Figure 11e,f).[101] By adjusting the width of the R6G strip on the graphene surface, ternary operations were achieved in MVL circuits. This capability allows higher data processing in a single material system, leading to a simplified integrated circuit design.

3.4.2. TMDCs Homojunctions

In 2017, Liu et al. uncovered the anti-ambipolar characteristics of multilayer MoS_2 under low temperatures (**Figure 12**a,b),[102] which contrasts with conventional AATs that always have heterojunction structures based on dissimilar materials. Through systematic investigation, it has been found that the anti-ambipolar features in MoS_2 arise from the inhomogeneous carrier distribution within the material. The near-substrate region exhibits p-doping, while the bulk region shows n-doping, leading to the observed anti-ambipolar behavior. The multilayer MoS_2 homojunction AATs device has the potential to simplify the device structure and circuit design when compared to conventional technology. Similarly, a multi-layer 2,6-diphenyl anthracene (DPA) organic semiconductor was also found to exhibit anti-ambipolar characteristics in 2018, attributed to the presence of a vertical potential barrier between the charge-accumulation interface and the neutral bulk.[160]

The polarity of transition metal dichalcogenides, such as WSe_2, usually depends on their thickness. In 2022, the monolayer and few-layer WSe_2 homojunctions exhibited anti-ambipolar switching behaviors because of the thickness-dependent band structure engineering and band offset at the vdW interface (Figure 12c,d).[104]

In addition to channel engineering in homojunction, dielectric engineering could also alter their electrical behaviors. The atomically thin 2D layered structure of semiconductors allows for engineering their electronic properties by manipulating the surrounding dielectric environment.[161] Impressively, by using stepped h-BN gate dielectric, anti-ambipolar WSe_2 transistors could generate two or more NDT regions in their transfer characteristic curves depending on step numbers (Figure 12e,f).[103] This work shows a straightforward way to increase the radix of MVL circuits (e.g., ternary, quaternary, and quinary inverters) by

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adding the dielectric regions with different thicknesses. In 2022, gallium ions (Ga^+) implantation was proved to be able to regulate the h-BN dielectric properties with a maximum surface potential difference of 1.3 V,[108] which induces the dominant p-type transfer characteristic in $MoTe_2$ channel that stacked on Ga^+-treated h-BN insulting layer due to a bandgap renormalization effect.[161] More importantly, such a dielectric engineering approach with high spatial selectivity was used to construct a $MoTe_2$ junction based on a single flake, by which the typical anti-ambipolar Λ-shaped behaviors are displayed in the junction transistors.

3.4.3. Si Homojunctions

The accumulated scientific knowledge on Si offers a good foundation for rapid innovations to achieve remarkable Si-based anti-ambipolar characteristics.[162,163] In 2017, high-performance Si-based AATs devices were successfully fabricated using a CMOS-compatible device fabrication process. These devices were based on p^+-i-n^+ Si ultrathin body transistors and exhibited distinct Λ-shaped transfer characteristics while operating at room temperature.[164,165] The anti-ambipolar behaviors, including a PVR above 10^4 and a SS of 70 mV dec^{-1} at the Λ-shape NDT peak region, are fully explained by the effectively gate-modulated junction characteristics.[164] The authors also calculated the RC time constant to be ≈0.1 µs and proposed that using high-mobility nano-channel device architectures could improve the speed limit of Si-based AATs circuits.[166] These works offer promising ways to obtain Si AATs-based multivalued logic with low power and high speed.

Furthermore, the Si ellipsoidal quantum-dot transistors can exhibit Λ-shaped negative differential transconductance (NDT) characteristics when the nanowire diameter exceeds 5 nm. Conversely, for nanowires with a diameter of less than 5 nm, these transistors demonstrate M-shaped Coulomb blockade characteristics.[167] These phenomena arise due to the presence of multiple tunnel barriers and quantum states within the Si nanowire.[168,169] This finding is meaningful for the room-temperature implementation of silicon quantum devices in reconfigurable MVL circuits beyond conventional binary-digital-logic technology.

3.5. Other Heterojunctions

Incorporating 3D semiconductors in vdW 2D/3D heterojunction systems offers a notable advantage of simplified processing. This advantage is due to their compatibility with diverse physical or chemical vapor deposition methods widely employed in traditional integrated-circuit fabrication techniques. On the other hand, unlike the strict requirements to achieve abrupt semiconducting 3D/3D heterojunctions with opposite doping polarities, 2D materials with layered crystal structures offer exceptional opportunities for developing 2D/3D anti-ambipolar heterojunctions and devices.

In 2016, Wang et al. demonstrated 2D/3D heterojunctions utilizing sputtered p-type SnO film and exfoliated n-type MoS_2 layers.[56] The p-SnO/n-MoS_2 heterojunctions show good diode rectification ratio up to 10^4 and anti-ambipolar characteristics depending on MoS_2 thickness. Surface potential mapping of p-SnO/n-MoS_2 heterojunctions was achieved using electrostatic force microscopy, suggesting a geometry-dependent current-flow model.

A narrow bandgap n-type semiconductor, InAs, was integrated with 2D BP material to create a heterojunction with broken gap band alignment.[170] Because of the narrow bandgap of two components, the BP/InAs heterojunction showed gate-tunable band-to-band tunneling and NDT behaviors with a narrow tunneling window of ≈0.1 V. Based on the similar 2D/3D integration concept, p-WSe_2/n-ZnO,[153] p-BP/n-ZnO,[171] p-MoS_2/n-ZnO,[172] and p-$MoTe_2$/n-IGZO[173] were combined by the different research group to show ambipolar carrier transport, by which high-gain inverter and frequency doubling circuits were successfully demonstrated.

By simply coating ZnO quantum dots on boron-doped silicon, vertical ZnO/p-Si heterostructure was formed with room-temperature NDR characteristics,[174] which results from the band-to-band tunneling and diffusion current. The NDR behavior of ZnO/p-Si heterostructure was also comprehensively investigated based on the energy band state and chemical structure of ZnO quantum dots with a morphological variation.

4. Devices

4.1. Optoelectronics

AATs are promising as optoelectronic components with exceptional photoresponse performance, multi-terminal regulation, and intelligent photodetection capabilities. Their good optical absorbance properties and diverse material combinations have led to exploring various optoelectronic coupling effects in AATs-based device optoelectronics.

4.1.1. 2D Material-Based Optoelectronics

With a practical photoinduced doping approach developed in 2019, the AATs performance of $MoTe_2/MoS_2$ heterojunction was successfully adjusted by manipulating the doping level (**Figure 13a**).[75] The type-II band alignment and high built-in potential in $MoTe_2/MoS_2$ heterojunction facilitate an energy conversion efficiency of 0.55% and a fill factor (FF) of 0.35 when utilized as a photovoltaic device (Figure 13b). When considering it as a self-powered photodetector device, a photoresponsivity of ~0.25 A/W, an EQE of 56%, and a response time of 2 ms were obtained under 600 nm light illumination (Figure 13c).

In a subsequent study, Hu et al. demonstrated the effective gate tunability of the photocurrent using the anti-ambipolar $MoTe_2/MoS_2$ heterojunction in 2019.[76] The researchers utilized rapid thermal annealing treatment to optimize the p-type doping level in $MoTe_2$, thereby modifying the electronic structure of the heterojunction. As a result, the heterojunction displayed tunable photocurrent across a significant gate-bias range from −60 V to 60 V, which is crucial for practical applications. Such tunability facilitates efficient modulation of photoresponse gain and on/off state, satisfying specific application requirements. Besides, working in a self-powered mode, the thermal-treated

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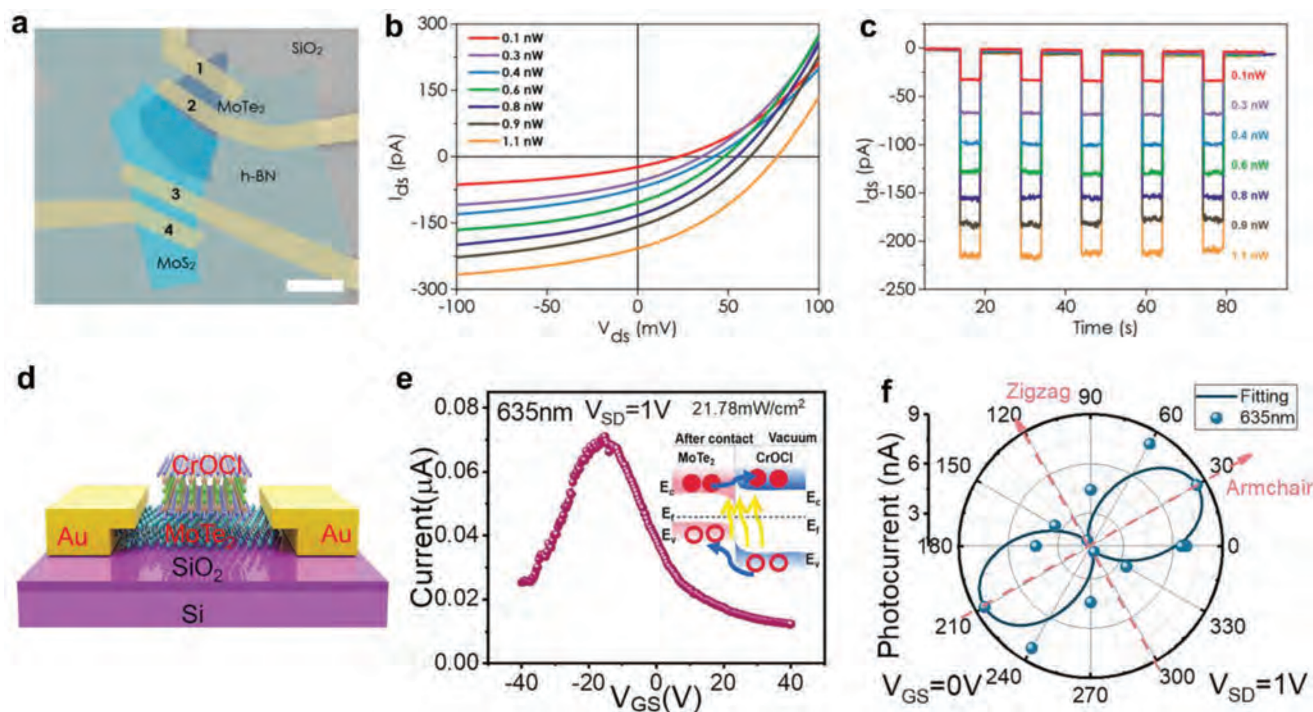

Figure 13. Photovoltaic device and polarization-sensitive photodetection. a) Device illustration, b) *I–V*, and c) *I–T* characteristic curves of the photovoltaic $MoTe_2/MoS_2$ heterojunction devices.[75] d) Schematic diagram and e) Λ-shaped transfer curves of the CrOCl/2H-$MoTe_2$ heterojunction AATs under light illumination.[79] Inset of e) shows the band structure of heterojunction under light illumination. f) Polar plots of polarization-resolved photocurrent. a–c) Reproduced with permission.[75] Copyright 2019, American Chemical Society. d–f) Reproduced with permission.[79] Copyright 2023, AIP Publishing.

anti-ambipolar $MoTe_2/MoS_2$ heterojunction showed a photoresponsivity of ~0.135 A/W and a photoresponse time less than 2 ms when illuminated at 532 nm light.

In 2022, a light-regulated AATs was built based on a simple metal-WSe_2-metal configuration by Wang et al.[105] The anti-ambipolar transport is mainly influenced by the dual contact barriers and photo-excited carriers. When light illumination with different incident powers is applied, the Λ-shaped transfer curves would be modulated accordingly. The metal-WSe_2-metal AATs exhibited excellent photodetection performances, such as a responsivity of 1.10 A W^{-1} (4.83 A W^{-1}) and a detectivity of 1.52×10^{10} Jones (6.94×10^{10} Jones) at 405 nm (635 nm) laser illumination. Following a power law, the photocurrent as a function of light intensity could be fitted by equation $I_{ph} \propto P^{\alpha}$.[98,175] The fitting factor α was determined as ≈0.75, suggesting a low recombination rate.[63,175] The photocarrier could regulate the anti-ambipolar switching characteristics of AATs, showing a new concept for multivalued logic/digital electronic and optoelectronic applications.

Polarization-sensitive photodetection of the incoming light has important applications in different technologies such as astronomy, quality assessment, and ellipsometry.[81,176,177] Most recently, an AAT based on CrOCl/2H-$MoTe_2$ heterojunction was designed to show polarization-sensitive photodetection (Figure 13d).[79] Here, the primary operating mechanism for the anti-ambipolar and polarization-sensitive photoresponse is based on the gate-tunable band bending and charge transfer at the CrOCl/2H-$MoTe_2$ interface. (Figure 13e). The anisotropic 2D CrOCl with intrinsic linear dichroism allows the heterojunction device to detect the polarization of the incoming light.[178] The CrOCl/2H-$MoTe_2$ heterojunction also shows good photodetection performance with a photocurrent dichroic ratio of ≈6 (Figure 13f), a responsivity of 1.05 A/W, and a photoresponse time of 970 µs.[79] Also, based on two strong anisotropic 2D materials, anti-ambipolar heterojunctions made by p-BP and n-ReS_2 show a more substantial linear polarized photocurrent ratio of 31.[126] It is promising that combining AATs with polarization-sensitive photodetection could enrich the optoelectronic device functionalities.[81]

Broadband photodetection can be realized through the design of anti-ambipolar heterojunctions.[19,98] Most recently, visible-near infrared (ranging from 520 to 2000 nm) photodetector was reported based on a vdW stacked $MoTe_2$/BP heterojunction (**Figure 14a**).[68] By applying appropriate gate and drain voltages, the transition between type-I and type-II band alignment can be achieved. This enables the dynamic tuning of conduction polarity, anti-ambipolar behavior, and photodetection performance. Under a self-powered operation mode, the built-in potential at the $MoTe_2$/BP interface enables efficient separation of photogenerated electron-hole pairs. This results in a responsivity of 290 mA W^{-1}, an EQE of 70%, a photoresponse time of 78 µs, and the achievement of broadband photodetection (Figure 14b).[68]

4.1.2. Organic Material-Based Optoelectronics

Organic AATs offer an advantage over their 2D counterparts since they can serve as both light absorbance and light irradiation

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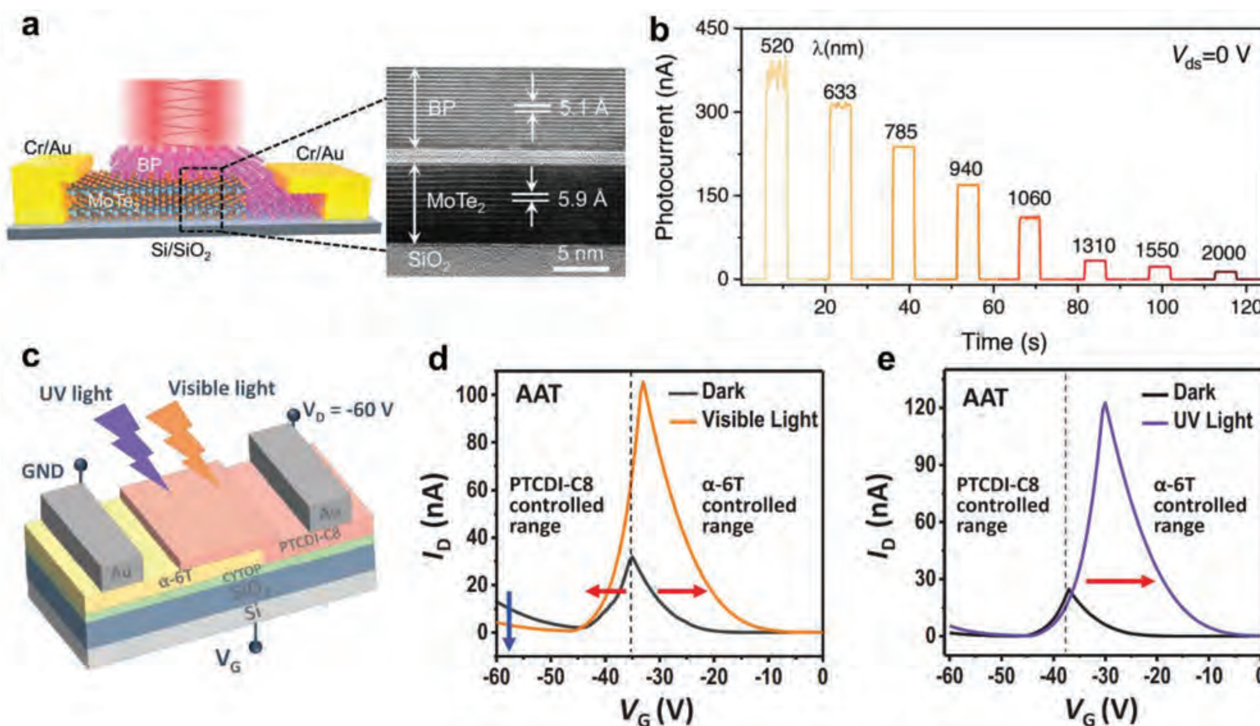

Figure 14. Broadband photodetection and organic photodetectors. a) Device architecture and cross-sectional HRTEM image of $MoTe_2$/BP heterojunction. b) Wavelength-dependent photocurrent of $MoTe_2$/BP heterojunction without bias voltage.[68] c) Schematic illustration of organic anti-ambipolar phototransistors comprising $\alpha-$6T and PTCDI-C8 layers. Transfer characteristics of organic anti-ambipolar $\alpha-$6T/PTCDI-C8 phototransistors under d) visible light and e) UV light irradiation.[179] a,b) Reproduced with permission.[68] Copyright 2023, Wiley-VCH. c–e) Reproduced with permission.[179] Copyright 2021, Wiley-VCH.

components. Furthermore, in organic anti-ambipolar heterojunctions, optical signals can facilitate optoelectronic multifunctional operations beyond simple photodetection capabilities.

Recently, it has been reported that light irradiations with different wavelengths were utilized to tune the transfer characteristics of organic p-6T/n-PTCDI-C8 heterojunction AATs (Figure 14c).[179] These organic semiconductors were selected based on their distinct photoresponse to light irradiation. Visible light has the significant effect of broadening the Λ-shaped transfer curves of such organic AATs (Figure 14d), whereas shifting is observed exclusively within the $\alpha-$6T controlled antihole range (Figure 14e). Based on the differential photoresponse of AATs to UV and visible light, the voltage transfer characteristics (VTC) of organic-based MVL circuits were precisely manipulated by applying appropriate optical inputs. Similarly, in 2023, Panigrahi et al. presented an optically controllable ternary device based on a p-type C8-BTBT/n-type PhC2-BQQDI heterojunction.[180] The characteristic spectral photoresponse of organic semiconductors allows the incident visible light to initiate programming operations, while UV light induces erasing operations.

Also, location-dependent multi-parameter detection behaviors were also explored in organic p-DNTT/n-PTCDI-C13 anti-ambipolar phototransistors based on a Schottky barrier-limited carrier injection.[82] Unlike conventional phototransistors that only capture limited incident light information, the AATs-based phototransistor offers a wealth of information regarding various sensing parameters, including incident location, light wavelength, and light-absorbing material. The irradiation locations were also proved to alter the Λ-shaped transfer curves because the AATs channel has a partially overlapping pn-heterojunction (DNTT and PTCDI-C13). This sensing scheme is expected to enable the advancement of intelligent photodetection.

Organic semiconductors have saturated bonds on their surface, enabling integration with other dangling bond-free materials through vdW interactions. This characteristic promotes efficient carrier transport and anti-ambipolar operations in organic-inorganic heterojunctions. For this purpose, Joo et al. fabricated AATs based on the hybrid rubrene/MoS_2 heterojunction,[90] revealing a gate bias-dependent photovoltaic effect under 532 nm laser irradiation. The photovoltaic AATs were operated in a self-powered mode, driven by light irradiation at the p-n heterointerface. Photocurrent mapping demonstrated that the rubrene/MoS_2 heterointerface exhibited the peak photocurrent and photovoltaic effect. The built-in potential and type-II band alignments induce the photovoltaic effect, as evidenced by several similar studies, such as p-WSe_2/n-WS_2[122] and pentacene/MoS_2 heterointerfaces.[55] These results suggest that AATs can be used as self-driven optical switches or novel types of optoelectronic interconnection devices.

4.1.3. Mixed-Dimensional 1D/2D Optoelectronics

In optoelectronic configurations, 1D/2D heterostructures typically exhibit enhanced light absorption attributed to the antenna effects of 1D nanowires.[146,181,182] **Figure 15a** displays an

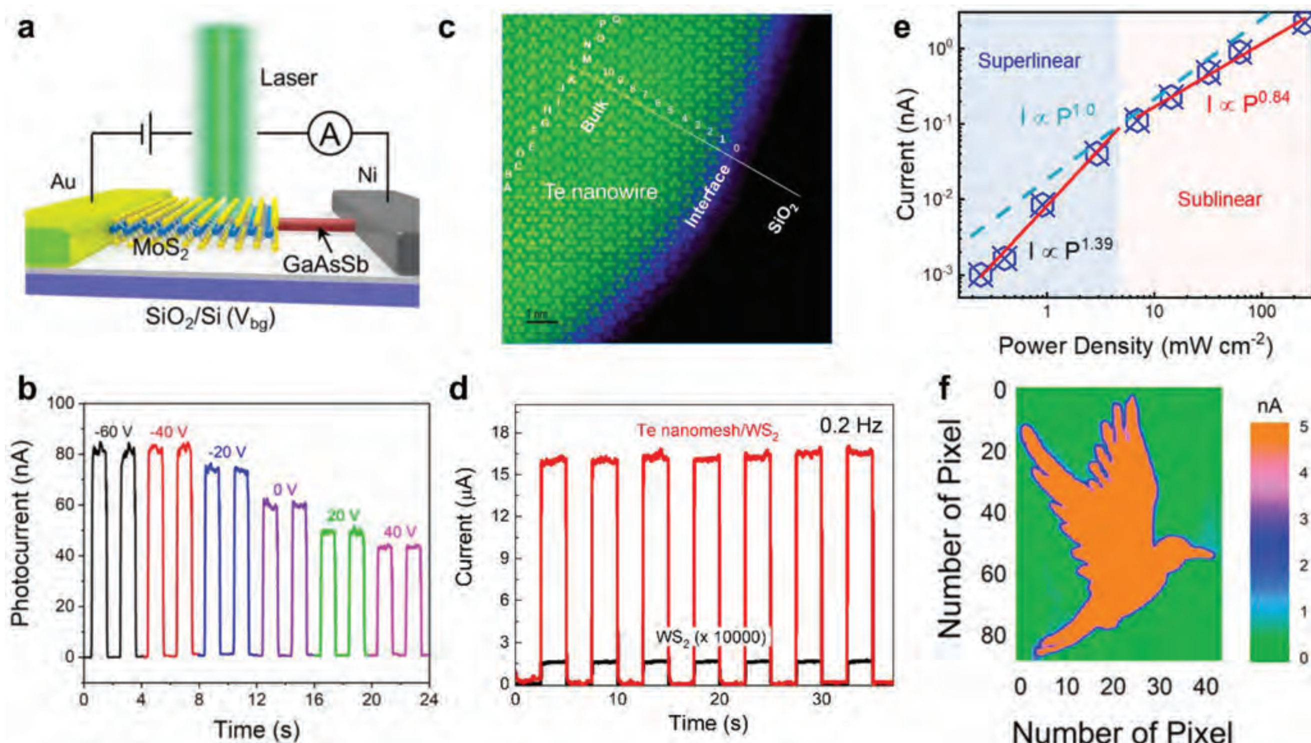

Figure 15. Mixed-dimensional 1D/2D optoelectronics. a) Device schematic of the 1D GaAsSb/2D MoS_2 heterojunction phototransistor and b) the photoresponse under different gate voltage.[98] c) Cross-sectional HAADF-STEM image of Te nanowires grown on SiO_2 via multi-scale vdW interactions.[57] d) Photodetecting performance of Te/WS_2 heterostructures under 532 nm irradiation. e) Superlinear and sublinear photoelectric conversion phenomenon of full-vdW 1D Te/2D Bi_2Se_2O photodiodes.[19] f) High-resolution image sensing based on GaAsSb/MoS_2 phototransistor. a,b,f) Reproduced with permission.[98] Copyright 2022, American Chemical Society. c,d) Reproduced with permission.[57] Copyright 2023, Springer Nature. e) Reproduced with permission.[19] Copyright 2022, Wiley-VCH.

illustration of the GaAsSb/MoS_2 phototransistor, where an n-type MoS_2 nanoflake was stacked on top of the p-type GaAsSb NW through vdW integration.[98] The anti-ambipolar rectification, light irradiation, and electrostatic field enable the multi-element regulated smart photodetection (Figure 15b). The theoretical basis for the tunability of photoresponse is related to the role of bending slope and depletion extension. This tunability enables greater integration freedom for anti-ambipolar phototransistors, enriching their advanced functionality and broad applicability.

Recent advancements indicate that further reducing the dimensionality of vdW materials, transitioning from 2D vdW monolayers to 1D vdW atomic chains, holds great promise as it approaches the ultimate limit of material downscaling, offering exciting prospects.[61,183,184] 1D Te vdW nanowires are free of dangling bonds, promising nanometers, and even sub-nanometer electronics.[185] Li et al. reported that Te nanowires could be grown directly on the MoS_2 surface, forming anti-ambipolar heterostructures through vdW epitaxy.[186] This strong vdW interfacial coupling induces an ultrahigh photoresponsivity above 10^3 A/W at the 1550 nm telecommunication wavelength.

Most recently, a different growth mechanism of 1D Te nanowires on different surfaces (including layered vdW material surfaces) at low temperatures was proposed by Meng et al. in 2023, namely multi-scale vdW interactions (Figure 15c).[57] The growth process at a low temperature of 100 °C does not compromise the material properties of the Te nanowire/WS_2 monolayer heterostructures. Following the successful construction of Te/WS_2 heterojunctions, their photoelectric performance was investigated (Figure 15d), yielding a photoresponsivity of 566.7 A/W, a response time down to 3 μs, and a cutoff frequency of 100 kHz. The good compatibility between the target device substrate and the Te nanowire growth process allows for the fabrication of devices on various technologically functional surfaces, enabling multifunctional mixed-dimensional optoelectronic applications.[57]

In another work, mixed-dimensional full-vdW 1D Te/2D Bi_2O_2Se photodiodes revealed a superlinear photoelectric conversion from the in-gap trap-assisted recombination (Figure 15e).[19] The hybrid full-vdW 1D/2D interactions can be formed with naturally terminated dangling-bond-free vdW interfaces, thus contributing to efficient carrier charge transport and anti-ambipolar modulations.[187] Owing to the high sensitivity of 1D/2D anti-ambipolar heterostructures, their applicability of image sensing was demonstrated with high-resolution and good operation stability (Figure 15f).[63,98]

4.2. Frequency Modulation

A critical characteristic of AATs is their ability to exhibit both positive and negative transconductances, which can be effectively

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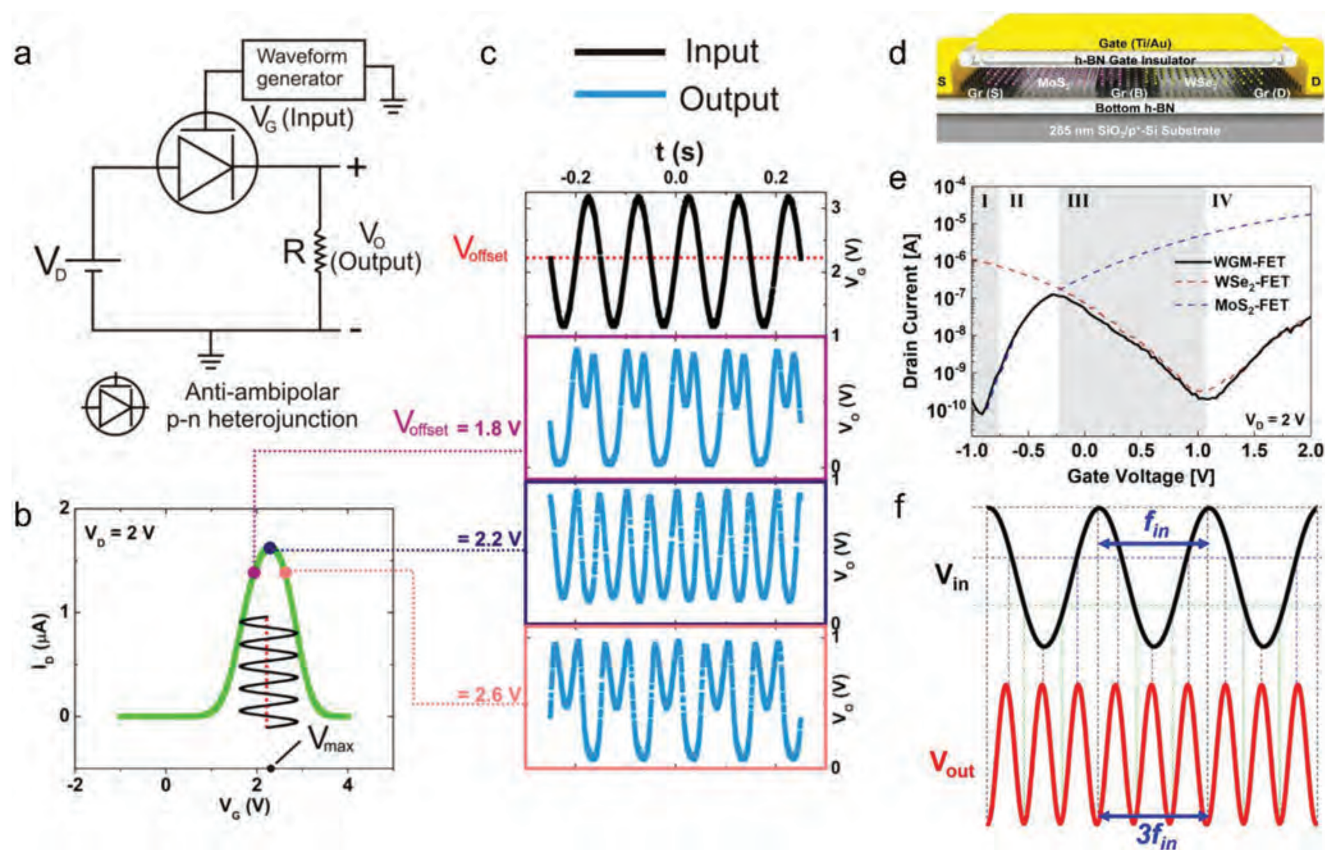

Figure 16. Frequency multiplying functions. a) Frequency doubling circuit utilizing SWCNT/a-IGZO anti-ambipolar heterojunctions.[93] b) Representative transfer characteristics of anti-ambipolar heterojunctions. c) (c) Input-output signal relationships with different offset voltage. d) Device schematic and e) transfer curves of the WSe_2-Gr-MoS_2 heterojunction AATs.[188] f) Input-output signal of frequency tripler based on WSe_2-Gr-MoS_2 heterojunction. a–c) Reproduced with permission.[93] Copyright 2015, American Chemical Society. d–f) Reproduced with permission.[188] Copyright 2023, Springer Nature.

utilized in analog signal modulation circuits, including frequency doubling, phase shifting, and frequency mixing.[97]

4.2.1. Frequency Multipliers

Frequency multipliers are generally built from a nonlinear electronic component by which the output frequency is a multiple of its input frequency.[189,190] AATs can be used for designing frequency multipliers, which are used in frequency synthesizers and communications circuits.[191,192] Using an AATs-based frequency doubler as an illustration, when an anti-ambipolar device is biased at an offset voltage equal to V_{peak}, the output signal (i.e., source-drain current) oscillates at twice the frequency of the input signal (i.e., gate voltage).

In 2014, a frequency doubling circuit was built using SWCNT/a-IGZO AATs (**Figure** 16a–c).[93] The power spectral purity of the frequency-doubling output signal is around 95%, exceeding the performance of graphene-based frequency doublers.[191,193] Based on the anti-ambipolar devices, frequency doubling circuits have been uncovered based on 2D $MoTe_2/MoS_2$ heterojunction in 2020 (Figure 16d–f). The resulting frequency doubler operates well with a cutoff frequency of 3 kHz. An AATs-based frequency multiplier, utilizing a single heterostructure device, greatly reduces the number of devices needed to achieve frequency modulation functions compared to conventional CMOS counterparts.[194]

Further device structure simplification could be realized by using homojunctions that avoid the utilization of dissimilar semiconductors. For example, frequency doublers have been successfully fabricated based on a single multi-layer DPA organic transistor or a single multi-layer MoS_2 transistor connecting with a resistor.[102,160]

Since 2009, the ambipolar graphene FETs have been leveraged to construct highly efficient frequency doubler devices.[191–193] Interestingly, Lee et al. successfully demonstrated frequency tripler circuits most recently, using laterally series-connected ambipolar WSe_2/Graphene/n-type MoS_2 channel AATs that feature with N-shaped transfer curves.[188] Device refinements, including device dimension reductions and local gate implementation, will improve the performance of the AAT-based frequency multiplier, enabling higher operating frequencies.

4.2.2. Phase Shift Keying

Moreover, the anti-ambipolarity can be utilized to implement more complex analog signal processing circuits. The primary

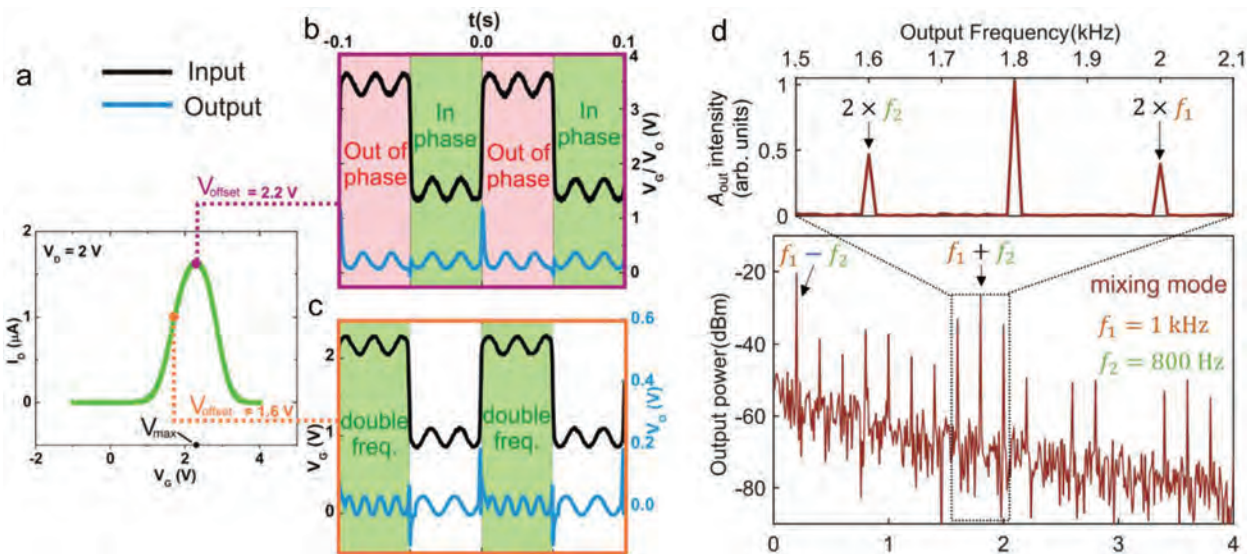

Figure 17. Signal processing and frequency mixing. a) Transfer characteristics of SWCNT/a-IGZO anti-ambipolar heterojunctions.[93] b) Phase shift keying and c) frequency shift keying functions of SWCNT/a-IGZO AATs. d) The power spectrum of vertical nanowire tunnel FET in frequency mixing mode. a–c) Reproduced with permission.[93] Copyright 2015, American Chemical Society. d) Reproduced with permission.[97] Copyright 2023, Springer Nature.

function of the phase shift keying (PSK) circuit is to modulate the AC signal with no phase shift for digital 0 transmission and a 180° phase shift for digital 1 transmission. PSK circuits are widely used in telecommunications and wireless data transmission technologies.[195,196]

Using a similar circuit configuration to the frequency doubler, just changing the input offset voltage could enable the operation of PSK (**Figure 17a**). Based on a fully solution-processed SWCNT/a-IGZO anti-ambipolar heterojunctions, the output sine wave maintains the same phase as the input wave when the square wave is in the low state (0 state). However, when the square wave is in the high state (1 state), the output sine wave experiences a 180° phase shift. (Figure 17b).[93] Featuring reducing fabrication complexity, an electrostatically controlled WSe2 homojunction transistor with reconfigurable anti-ambipolar characteristics also demonstrated the PSK functions.[106]

4.2.3. Frequency Shift Keying

Furthermore, the binary frequency shift keying (FSK) circuit accomplishes doubling the AC signal frequency solely when the square wave is in the high state (1 state). The binary FSK circuit is a specific frequency modulation type utilized in microwave radio and satellite transmission systems.[102,197]

Additionally, by making further adjustments to the amplitude of the input square wave, the binary FSK function can be demonstrated in SWCNT/a-IGZO anti-ambipolar heterojunctions (Figure 17c).[93] Unlike conventional Si integrated circuit technology, which utilizes a Gilbert cell comprising three pairs of emitter-coupled transistors to achieve these frequency multiplying functions,[198] the AATs-based frequency modulation circuits only necessitate one anti-ambipolar heterojunction connected in series with a single load resistor. This integration simplifies the corresponding circuit design significantly.

4.2.4. Frequency Mixing

Another essential signal modulation operation facilitated by AATs devices is frequency mixing, which generates new signals corresponding to the sum and difference frequencies of the original input signal. The frequency mixer is extensively utilized in wireless communications and plays a vital role in both frequency up-conversion for transmitters and frequency down-conversion for receivers. Typically, when the signal consists of two different frequencies (f_1 and f_2) input, multiple output frequencies (e.g., f_1-f_2, $2f_1$, f_1+f_2, and $2f_2$) could be generated.[199]

Most recently, in 2023, a frequency mixer based on reconfigurable vertical nanowire tunnel FET was reported by Zhu et al.,[97] by which two-analog-signal frequency mixing is performed on two input signals with $f_1 = 1$ kHz and $f_2 = 800$ Hz. The mixing power spectrum shown in Figure 17d reveals that a significant portion of output power (≈90%) is concentrated at frequencies f_1-f_2 and f_1+f_2. This observation indicates exceptional spectral purity and minimal undesired harmonics, making the device suitable for frequency down-conversion and up-conversion applications.

4.3. Synaptic Devices

Inspired by biological synapses, the logic-in-memory architecture combines logic and memory components into a unified artificial synaptic device (**Figure 18a**).[200–202] This architecture aims to address the von Neumann bottleneck caused by the physical separation of data processing and memorization units, offering significant potential to improve data processing capacity and reduce power consumption.

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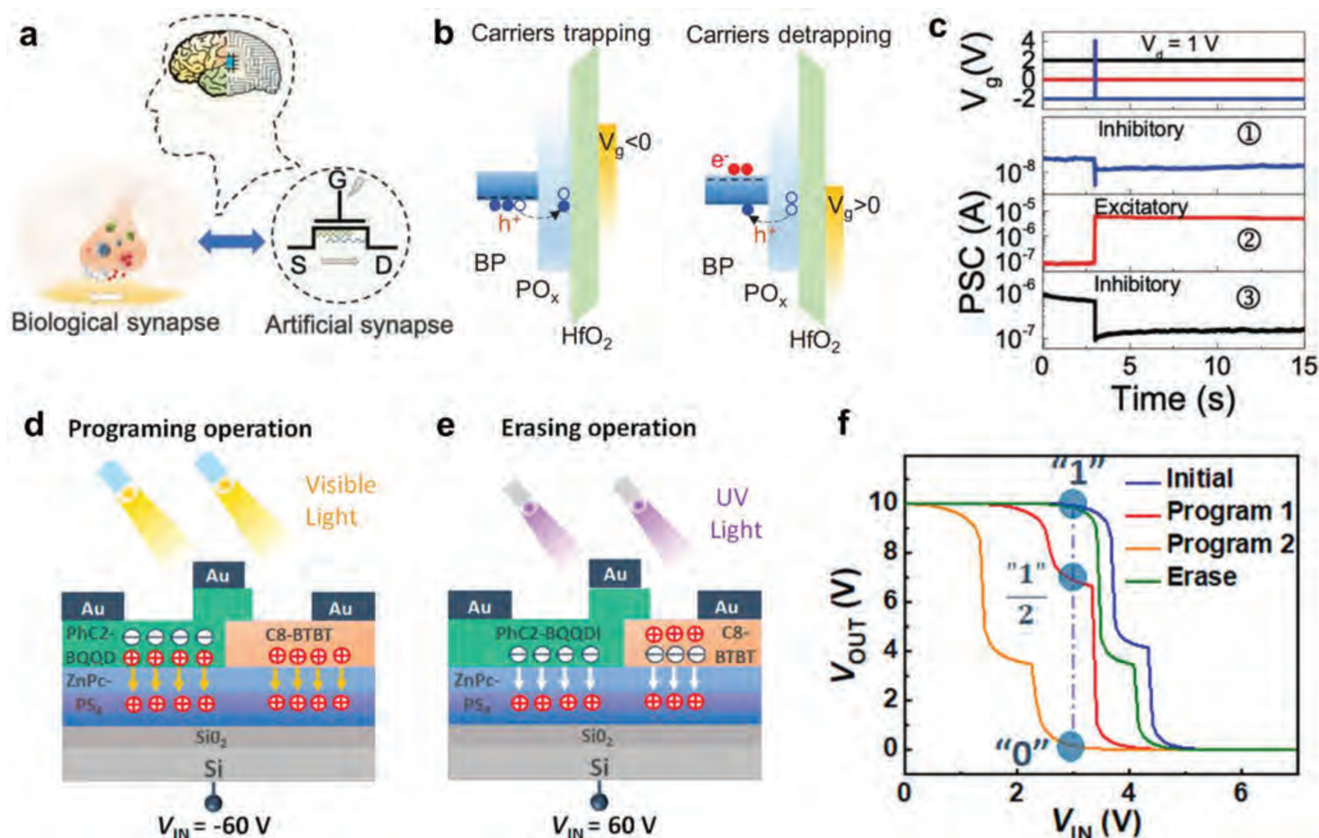

Figure 18. Logic-in-memory devices. a) Schematic diagram of biological and artificial electronic synapses. b) Schematic band diagrams for carriers trapping and de-trapping processes in BP/ReS_2 heterojunction and c) their synaptic behavior under different bias conditions.[67] d,e) Device illustration, and f) optically controlled program/erase operations of organic C8-BTBT/PhC2-BQQDI heterojunction.[180] a–c) Reproduced with permission.[67] Copyright 2020, Wiley-VCH. d–f) Reproduced with permission.[180] Copyright 2023, American Chemical Society.

4.3.1. Electronic Synapses

Based on the reported non-volatile memory performance and high program/erase ratio of $\approx 10^9$,[18,203] 2D vdW heterojunctions hold great potential to form multifunctional logic-in-memory devices. In 2020, Xiong et al. reported a vdW BP/ReS_2 heterojunction-based anti-ambipolar device for nonvolatile MVL operations.[67] The natural oxidation of BP forms an ultrathin defective phosphorus oxide layer (PO_x), which serves as the charge tunneling/trapping layer (Figure 18b).[204,205] The postsynaptic current of the BP/ReS_2 heterojunction synaptic device exhibits both excitatory and inhibitory synaptic behaviors under different bias voltages (Figure 18c). Building upon these characteristics, the research showcased the implementation of reconfigurable logic-in-memory and ternary logic operations, allowing for the regulation of logic states "1", "1/2", and "0" through input voltages.

In 2023, a sweep direction-dependent MVL inverter was built based on inkjet-printed SWCNT/In_2O_3 heterojunction AATs.[95] The demonstrated inverter showcases a logic-in-memory capability, enabling it to function in either ternary or binary mode depending on the direction of voltage sweeps. The VTC characteristics demonstrate the presence of three distinct logic states during the forward V_{IN} sweep direction, whereas the reverse V_{IN} sweep direction exhibits binary behavior. Notably, the device maintains stable operations even after being subjected to long-term constant bias stress and exposed to air for 4 days. The authors suggested that the sweep-direction dependent ternary/binary conversion is caused by the hysteresis characteristics of the load In_2O_3 FET and SWCNT/In_2O_3 heterojunction AATs.

4.3.2. Photoelectronic Synapses

Optically controllable logic-in-memory operations could achieve high data integration and enable optoelectronic multifunctional applications. In 2023, Panigrahi et al. utilized a p-type C8-BTBT/n-type PhC2-BQQDI heterojunction as a channel to establish optically controllable ternary logic-in-memory devices, while zinc phthalocyanine-cored polystyrene (ZnPc-PS4) layer function as the floating gate (Figure 18d,e).[180] The photo-induced hole-trapping ability of ZnPc-PS4 enables an optically controllable ternary data processing and storage system with a memory voltage window of 18 V. In the same work, a high-*k* HfO_2 dielectric was employed to low the operation voltage of logic-in-memory devices (Figure 18f), promising for energy-efficient electronics. To date, floating gate configurations have been generally studied in various memory or synaptic devices,[206–208] different material systems (e.g., metal nanoparticles-based and graphene-based

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floating gate) and operation mechanisms (e.g., hot-electron injection and Fowler-Nordheim tunneling) could be explored in AATs-based logic-in-memory devices in the future.[209,210]

Typically, the gate terminal or light irradiation acts as the presynaptic input terminal, whereas the source terminal serves as the postsynaptic output. The postsynaptic current (i.e., synaptic weight) exhibits excitatory or inhibitory responses upon presynaptic input, varying based on stimulation intensity, frequency, and duration. Up to now, the reported AATs heterojunctions-based neuromorphic devices have primarily operated based on the charge trapping and floating gate mechanisms.[67,95,180] In the future, researchers could explore and utilize diverse working mechanisms of artificial synapses, such as ion migration, dipole alignment, and conductive filament.[59,211] In addition to fine-tuning the basic synaptic connection strength in response to various excitatory and inhibitory states, researchers should aim to develop more sophisticated synaptic operations (e.g., spike-timing-dependent plasticity) and advanced brain-like functionalities (e.g., orientation selectivity and direction recognition) using AATs heterojunctions.[4,132,212]

5. Circuits

Multivalued logic circuits handle ternary, quaternary, or even higher-valued digital signals, offering promising architectures surpassing the fundamental bit limit, allowing for increased data storage density and developing more complex logic devices. In contrast to the existing binary von Neumann's architecture, these MVL circuits can overcome the inefficiency of physically separated processor/memory units.

The integration density of modern electronics has been dramatically enhanced in recent decades to improve data processing capabilities. This achievement has been facilitated by reducing the size of individual device components through advanced lithographic technologies. However, as the feature size of state-of-the-art transistors approaches its technical limit, challenges arise in further downsizing processes. Moreover, the subsequent substantial power consumption becomes a pressing concern, demanding the exploration of alternative approaches. It is well-established that integration density can be enhanced by increasing the number of logic states. For example, ternary inverters with N elements exhibit an exponential increase in integration density with a factor of 3N, resulting in significantly higher density than standard binary inverters (2N). In this context, anti-ambipolar transistors hold promise for constructing multi-valued logic systems that surpass conventional binary inverters.

In any numerical system, expressing a given quantity requires a smaller number of digits when the radix becomes larger. The digits needed to represent a range of N are determined by the equation $N = R^{\mathrm{d}}$ where R is the radix and d is the necessary digits. The circuit complexity (C) is directly proportional to the digit capacity ($R \times d$) as

$$C = k\ (R \times d) = k\left(R\frac{\log N}{\log R}\right) \tag{1}$$

By incorporating an additional state into a binary logic system, significant improvements in area efficiency can be achieved, resulting in a more than 35% reduction in unit devices and interconnect lines in a ternary logic system (**Figure 19**).[213] In the case of a quaternary logic system, this reduction percentage increases to 50%. Additionally, MVL circuits provide the advantage of reducing power consumption while enhancing processing speed.

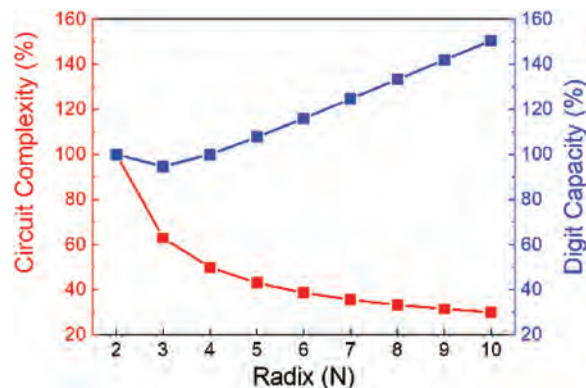

Figure 19. Estimation of the circuit complexity and digit capacity as a function of radix.

5.1. Ternary Inverters

A ternary inverter introduces an additional intermediate state, expanding the number of input or output logic states to three: "1", "1/2", and "0". In the 1990s, a family of ternary logic gates was designed based on CMOS technology, incorporating both depletion and enhancement types of transistors.[214] Nevertheless, the increased interconnections required to build basic logic functions presented substantial challenges to the binary-logic-based CMOS technology. Ternary inverters based on AATs provide the advantage of increased integration density and reduced device complexity compared to conventional binary logic gates. So far, AATs-based MVL circuits have been developed using diverse material combinations, such as 2D/2D, 2D/1D, organic-organic, and organic/inorganic semiconductor heterojunctions, as summarized in **Table 3**.

5.1.1. 2D Material-Based Ternary Inverters

The first 2D material-based ternary logic inverter was built on MoS_2/WSe_2 heterojunction in 2016.[17] As shown in **Figure 20**a,b, the ternary inverter circuit can be considered as a WSe_2 transistor in series with a parallel-mode MoS_2/WSe_2 transistor. With effective modulation of charge density and energy band, induced by the strong interlayer coupling between layered materials and the dielectric optimization (employing high-k HfO_2 dielectric), the MoS_2/WSe_2 heterojunction transistors show improved negative differential transconductance at room temperature (Figure 20c). When configuring into a ternary inverter, as shown in the VTC in Figure 20d, three distinct levels are obtained with a V_{dd} of 1 V, corresponding to three logic states of 1, 1/2, and 0, when V_{in} varied from 0 to 1 V. The MoS_2/WSe_2 heterojunction-based ternary inverter shows voltage gains of ≈4.5 and ≈2.5 for the first and second logic states, respectively.

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Table 3. Performance summary of AATs-based ternary inverters.

	AATs (p-/n-channels)	In-series Channels	Dielectrics	V_{DD} [V]	V_{IN} [V]	1st/2nd Gains	Notes	Reference
2D-based	WSe_2/MoS_2	WSe_2	HfO_2	1	0 to 1	4.5/2.5	First 2D ternary MVL	[17]
	WSe_2/MoS_2	WSe_2	SiO_2	8	−80 to −20	–	–	[43]
	WSe_2/MoS_2	WSe_2	SiO_2	–	−40 to 50	0.08/0.26	–	[71]
	WSe_2/graphene	WSe_2	SiO_2	4	−30 to 30		Light-triggered	[73]
	BP/MoS_2	BP	HfSiO	1 to 2	−1 to 1	12/8	Drain voltage tunable	[18]
	BP/MoS_2	BP	SiO_2	2	-−25 to −5	0.1/0.15	–	[124]
	BP/ReS_2	BP	SiO_2	1.6 to 2.0	15 to 30	1.7/2.2	Type-III alignment	[66]
	BP/ReS_2	BP	HfO_2	0.1 to 2	−4 to 2	–	Nonvolatile logic	[67]
	$MoTe_2/MoS_2$	$MoTe_2$	SiO_2	4 to 20	−60 to 60	0.5/1	Light tunable	[39]
	$MoTe_2/MoS_2$	$MoTe_2$	hBN/SiO_2	0.1 to 2	−40 to 40	0.1/0.2	Photoinduced doping	[75]
	$MoTe_2/MoS_2$	$MoTe_2$	hBN/SiO_2	2	−60 to 60	–	Device annealing	[76]
	$MoTe_2/MoS_2$	Resistor	PS/Al_2O_3	1 to 3	−5 to 2	2/10	–	[215]
Organic-based	$\alpha-$6T/PTCDI-C8	PTCDI-C8	Al_2O_3	10	0 to 4	–	First organic MVL	[16]
	$\alpha-$6T/PTCDI-C8	PTCDI-C8	Cytop/SiO_2	60	0 to 60	–	Optically tunable	[179]
	$\alpha-$6T/PTCDI-C8	PTCDI-C8	Al_2O_3	10	0 to 4	–	Full-swing operation	[38]
	C8-BTBT/PhC2-BQQDI	PhC2-BQQDI	PMMA/SiO_2	60	0 to 60	16/18	Optically tunable	[216]
	C8-BTBT/PhC2-BQQDI	PhC2-BQQDI	PMMA/HfO_2	12	0 to 10	23.4/37.5	First flexible MVL	[85]
	C8-BTBT/PhC2-BQQDI	PhC2-BQQDI	ZnPc-PS_4/HfO_2	10	0 to 7	–	Floating gate	[180]
	DNTT/PTCDI-C13	PTCDI-C13	SiO_2	50	0 to 50	13/20	Full-swing operation	[84]
	DNTT/TCDI-C13	PTCDI-C13	pV3D3	0 to 8	0 to 8	15/30	Asymmetric contact	[83]
	DNTT/PTCDI-C13	PTCDI-C13	pV3D3	5	0 to 5	24.2/4.8	3D stacking	[8]
1D-based	SWCNTs/In_2O_3	SWCNTs	HfO_2	2	0.5 to 2	–	Inkjet printing	[156]
	SWCNTs/In_2O_3	In_2O_3	HfO_2	1 to 3	0 to 4	5/11.4	logic-in-memory	[95]
	SWCNTs/In_2O_3	SWCNTs	HfO_2	1.35	−0.5 to 1.35	–	–	[96]
Homo-junctions	Graphene	Graphene	SiO_2	2	0 to 2	–	Charge transfer doping	[100]
	Graphene	Graphene	SiO_2	1	−40 to 50	–	Optical gating	[101]
	MoS_2	MoS_2	Al_2O_3	1	−6 to 12	–	Chemical Doping	[10]
	$MoTe_2$	$MoTe_2$	hBN/SiO_2	3 to 15	−60 to 60	–	hBN engineering	[108]

Later in 2016, using a similar circuit configuration, the ternary inverter was constructed using BP/ReS_2 heterojunction transistor as a driver and the BP p-channel FET as a load.[125] These pioneering studies of 2D materials-based ternary inverters represent an important step toward the AATs-based MVL circuits, inspiring intensive research interest in MVL applications using 2D vdW heterojunctions.

The tunable 2D materials-based ternary inverter was built on MoS_2/BP heterojunctions in 2017 (Figure 20e).[18] The electron affinity difference between MoS_2 and BP is only 0.1 eV, providing the opportunity to alter the energy band offset broadly. Interestingly, the transition between binary and ternary inverter was exhibited by simply adjusting the supply bias voltages (Figure 20f). Also, the bias voltages and channel lengths were used to change the status of the middle logic states, including their position and range, highlighting the high tunability and multifunctionality outperforming previous binary logic devices. Given the high-k HfSiO dielectric layers with high specific capacitance used in this work, the ternary inverters based on MoS_2-BP heterojunctions show high voltage gains of 12 and 8 for the first and second logic states, respectively, with a V_{dd} of 2 V. These voltage gains were better than the already reported 2D materials-based ternary inverter at that time.

The good light sensitivity of 2D semiconductors could be employed to alter their MVL circuit performance. In 2019, the operating modes of $MoS_2/MoTe_2$ heterojunction-based inverter were reported to be transformed from ternary to binary by employing laser irradiation.[39] different incident intensities, the photogenerated carriers could reduce the resistance of the MoS_2 channel to some content by which different logic states are available. When subjected to 405 nm laser irradiation at various incident intensities, the photogenerated carriers have the ability to decrease the resistance of the MoS_2 channel to a certain extent, thereby enabling different logic states. Also, in a photosensitive graphene p-n junction AATs partly optically gated by photosensitive dye R6G molecules,[101] the illumination power of incident light (550 nm) could influence the potential difference in the anti-ambipolar junctions, which in turn regulate the performance of the AATS as well as the ternary inverters.

5.1.2. Organic Materials-Based Ternary Inverters

The first organic ternary inverter was reported in 2018 by Kobashi et al.,[16] where the circuit configuration can be considered as a loading organic n-PTCDI-C8 transistor in series with a

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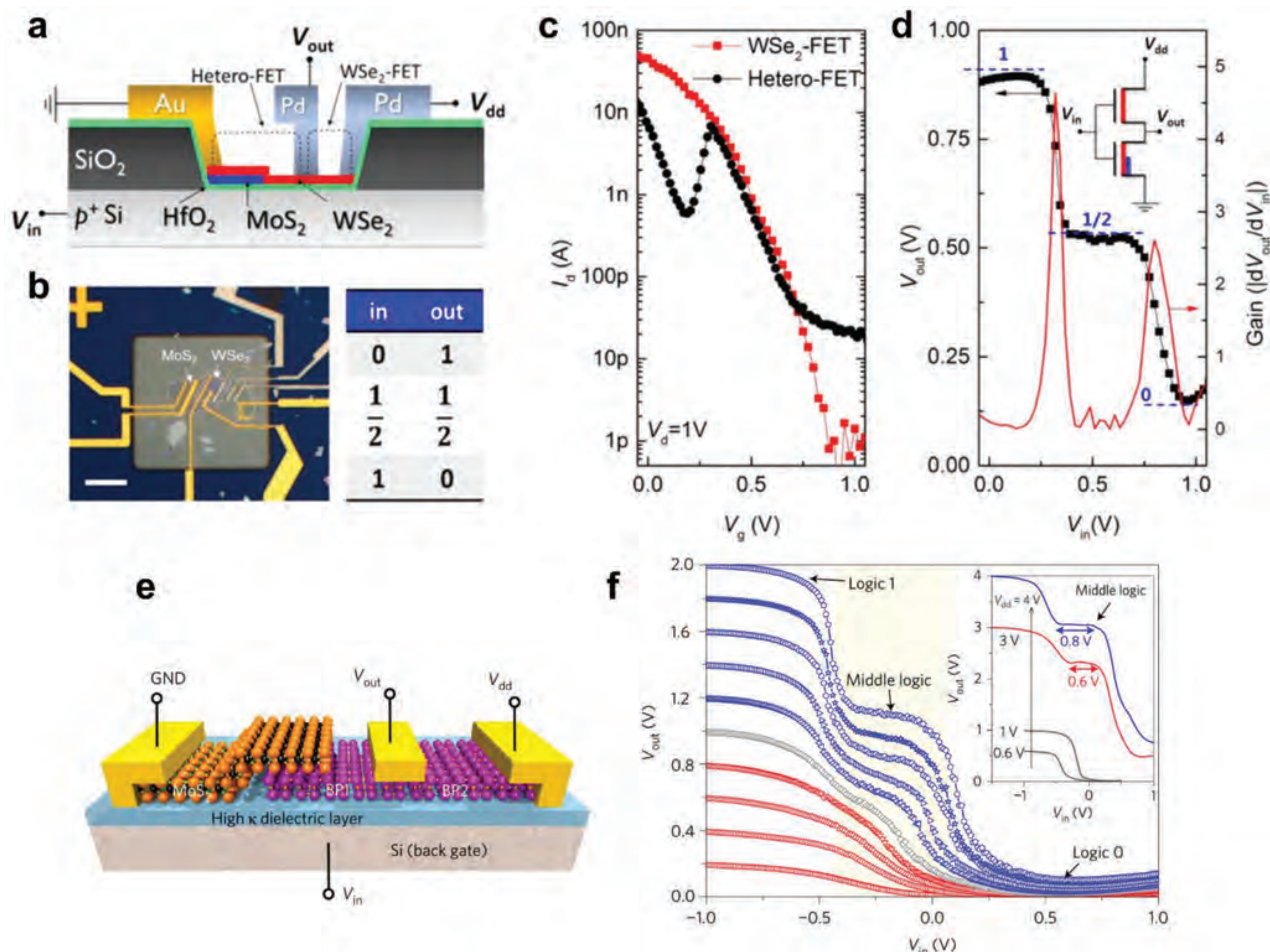

Figure 20. 2D materials-based ternary inverters. a) Schematic view, b) optical image, and truth table of the ternary inverter based on MoS_2/WSe_2 heterojunctions.[17] c) Transfer curves of MoS_2/WSe_2 heterojunction transistor and WSe_2 transistor. d) VTC characteristics of MoS_2/WSe_2 heterojunction-based ternary inverter showing three distinct logic levels. e) Schematic view of tunable inverters based on MoS_2/BP heterojunctions and f) their transition between binary to ternary inverter under different biases.[18] a–d) Reproduced with permission.[17] Copyright 2016, American Chemical Society. e,f) Reproduced with permission.[18] Copyright 2017, Springer Nature.

parallel-mode organic p-6T/n-PTCDI-C8 AAT fabricated by vacuum deposition (**Figure 21a**). The demonstration of three levels of output voltage ("0", "1/2", "1") is direct evidence of ternary inverter operation. In this case, the logic state ("0") was induced by the NDT characteristic of anti-ambipolar heterojunction. Given the excellent controllability of vacuum-deposited organic films, the device geometry engineering, such as channel length (from 300 to 550 μm) and channel thickness, are systematically designed to improve carrier injection (Figure 21b,c).[16,40] Note that gate-insulating layers with a higher dielectric constant (i.e., Al_2O_3 with $\kappa \approx 9$) can accumulate higher carrier density at channel/dielectric interface, which endows the ternary device with reducing operating voltage ≈35 V to ≈4 V.[217–219]

In the following work, interface engineering was applied to the channel/electrode interfaces and channel/dielectric interface, aiming to enhance the carrier injection and carrier accumulation, respectively.[20] Although the organic semiconductors-based ternary inverters hold promise as components of flexible circuits, it still presents imperfections, including unbalanced logic states, inadequate output swing, and a narrow noise margin.

Modifying the heterojunction transistor architecture could be a promising way to address these issues, thereby enhancing the operating frequency and lowering the energy consumption, along with the increasing switching gains of MVL devices. As an example, to address the nonideal asymmetric electrical characteristics in an organic p-type DNTT/n-type PTCDI-C13 heterojunction transistor, the DNTT channel was connected to both the source and drain electrodes, while the PTCDI-C13 channel made contact with only one of the electrodes (Figure 21d).[84] The AATs exhibited an N-shaped transfer curve due to the presence of a continuous p-channel, resulting in a subsequent increase in drain current above the NDT range with an increase in gate bias voltage (Figure 21e). This contributes to the full V_{DD}-to-GND swing in the VTC curves of the organic ternary inverter, whereas the first and second gain values were 13 and 20 V V^{-1}, respectively (Figure 21f). In the same work, a CYTOPs polymer layer was also deposited on the SiO_2 dielectric layer to reduce the electrical

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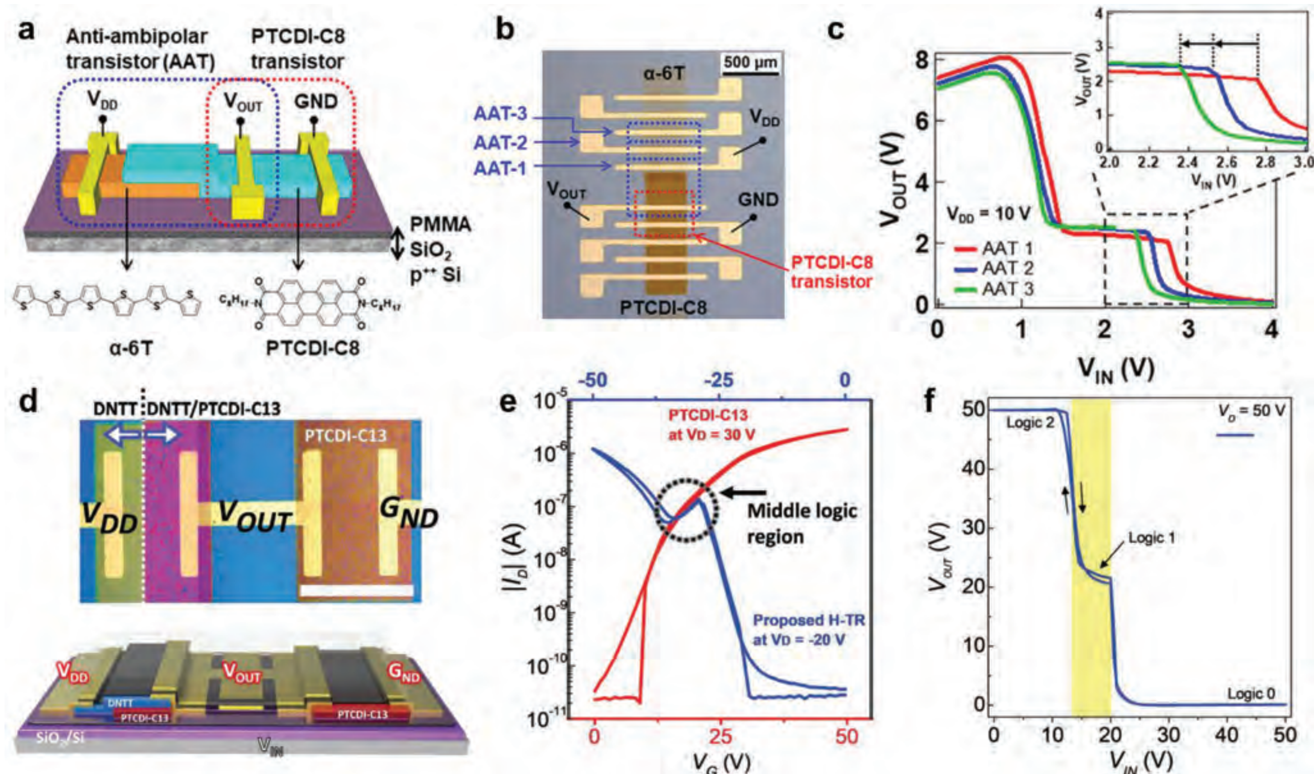

Figure 21. Organic materials-based ternary inverters. a) Schematic illustration, b) optical image, and c) VTC curves of organic ternary inverter with different channel lengths.[16] d) Optical image and schematic illustration of organic ternary inverter based on an n-type loading organic PTCDI-C13 transistor and an organic DNTT/PTCDI-C13 heterojunction AAT.[84] e) Transfer curves of DNTT/PTCDI-C13 heterojunction AAT and PTCDIC13 transistor. f) VTC characteristics of organic DNTT/PTCDI-C13 ternary inverter. a–c) Reproduced with permission.[16] Copyright 2018, American Chemical Society. d-f) Reproduced with permission.[84] Copyright 2019, Wiley-VCH.

hysteresis and improve reproducibility.[84] Enabled by the hysteresis-free full-swing operations of three-level VTC, the transient operation of a ternary inverter circuit based on organic DNTT/PTCDI-C13 heterojunction was demonstrated.

Using a device geometry engineering strategy, Lee et al. investigated the DNTT/PTCDI-C13 heterojunction AATs and their ternary inverter.[83] After systematically optimizing the asymmetric electrodes and the channel thicknesses, the carrier injection and transportation are well-adjusted to achieve high MVL performance with well-defined intermediate logic states. The status of the mid-logic plateau is highlighted as an essential figure-of-merit for a stable ternary inverter, as it characterizes the tolerance window of the intermediate ("1/2") state. In this work, the organic MVL circuits showed dramatically improved performance, including low operating voltage (< 8 V), full-swing operation, balanced logic states, high gains (15/30 for the first/second gains), and high static noise margin. The proposed asymmetric electrode architecture offers the potential to optimize the electrical characteristics of various types of AATs and their circuits without requiring modifications to the device design, fabrication process, or materials.

Due to their inherent mechanical flexibility, lightweight nature, and low-cost fabrication, flexible organic electronics are promising building blocks for future IoT devices.[131] This also recently attracted much research interest in mechanical flexible ternary inverters based on organic semiconductor materials.[46,83,85] In 2021, Panigrahi et al. reported the first flexible organic AAT and ternary inverter based on polyethylene naphthalate (PEN) substrate, as presented in **Figure** 22a,b.[85] In the organic heterojunction, PhC2-BQQDI and C8-BTBT were used as n-channel and p-channel, respectively. It is noted that the stacked poly(methyl methacrylate) (PMMA)/hafnium oxide (HfO_2) dielectric layer enabled low-voltage operation (max V_{in} is 10 V) and mechanical flexibility. The ternary inverter demonstrated stable and repeatable operation, even after undergoing 100 bending cycles (Figure 22c), as evidenced by the bending test (6.6 mm bending radius) and the mechanical durability.

Following that, Lee et al. presented a remarkably advanced flexible ternary circuit based on a PEN substrate (Figure 22d).[83] In this work, the DNTT/PTCDI-C13 heterojunction ternary inverter operated in full swing output voltage, together with significantly improved performances (Figure 22e), including balanced ternary logic states, better mechanical durability (2.4 mm bending radius) and high static noise margin.

5.1.3. Device Modeling of Ternary Inverters

Device/circuit modeling is helpful to understand the involved fundamentals in heterojunction areas and to obtain ideal ternary behavior.[220] It has been reported that optimizing the channel thickness and length was practicable to enhance the performance

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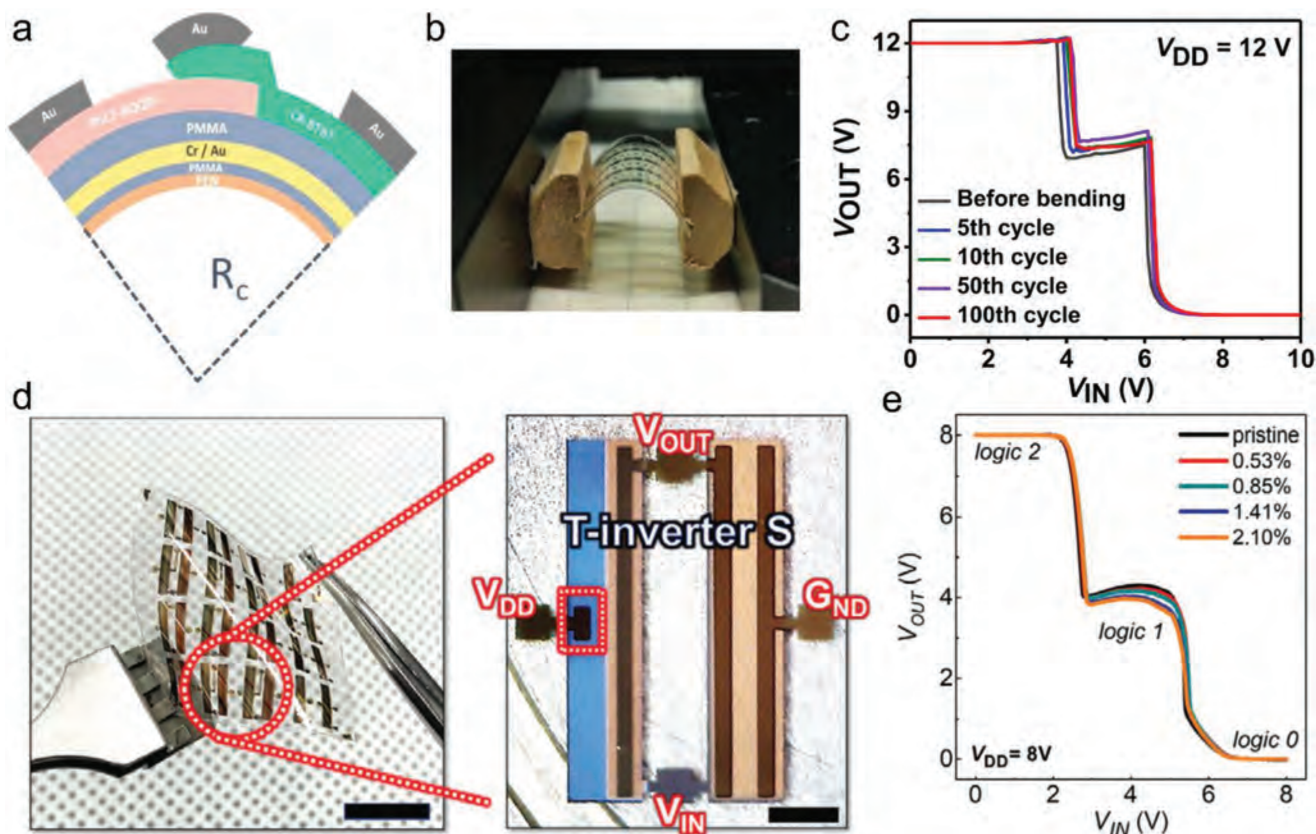

Figure 22. Mechanical flexible ternary inverters based on organic materials. a) Schematic illustration, b) photograph image, and c) VTC characteristics with different bending cycles of the flexible organic C8-BTBT/PhC2-BQQDI ternary inverter.[85] d) Photograph, optical image, and e) VTC characteristics with different tensile strains of the flexible organic DNTT/PTCDI-C13 ternary inverter.[83] a–c) Reproduced with permission.[85] Copyright 2021, IOP Publishing. d, e) Reproduced with permission.[83] Copyright 2021, Wiley-VCH.

of the organic-based ternary inverter.[34,38,41] In 2020, a finite-element simulation suggested that the junction energy barrier and minority carrier penetration play vital roles in improving the output swing and balancing the three voltage levels of the VTC.[34] The parametric simulations of the terminal characteristics and precise solutions of key physical quantities assist in explaining the complex three-level VTC.[221]

In 2021, a two-dimensional finite-element theoretical analysis was conducted on an organic 6T/PTCDI-C8 heterojunction-based ternary inverter with varying structural, materials, and interface parameters (**Figure** 23a,b).[38] This work proposes that the input-output characteristics can be finely controlled by the contact-depletion effect, channel length, semiconductor film thickness, carrier mobility, and contact barrier, with the goal of achieving a nearly ideal VTC. (Figure 23c–f). Until now, MVL physical simulations have only explored a limited range of materials and geometries, indicating the need for comprehensive multi-parametric investigations in the future.

5.2. Quaternary Inverters

As previously mentioned, incorporating an additional state into a logic system provides notable advantages in terms of cost efficiency, power efficiency, and the potential for high integration density. Recent progress in the transfer curves of AATs, particularly the achievement of double-peak M-shaped curves, is crucial for advanced MVL circuit design. This result reveals the significance of transfer curve engineering in fully utilizing the capabilities of AATs in quaternary logic circuits.[14,15,103,222]

5.2.1. 2D Material-Based Quaternary Inverters

In 2019, a full-vdW WS_2-graphene-WSe_2 heterostructure was applied to double-peak NDT device operations (**Figure** 24a,b).[15] With device configuration engineering, the two consecutive NDT phenomena are found to be controlled by the gate-tunable energy barriers of WS_2-graphene and graphene-WSe_2 heterojunctions. In 2020, a double NDR characteristic was uncovered by Jung et al. in a 2D/organic tunneling device comprising two HfS_2/pentacene heterojunctions and one vertical organic pentacene resistor.[223] In 2022, a p-i-n WSe_2 homojunction AAT was fabricated to achieve double NDT characteristics, with PVR values of 36.6 and 12.9.[224]

The charge transfer doping was applied on a homogeneous bilayer WSe_2,[225–227] by which the sequentially located n-doped (induced by cross-linked PMMA), intrinsic, and p-doped (induced by Au_2Cl_6) WSe_2 regions were achieved. Through experimental

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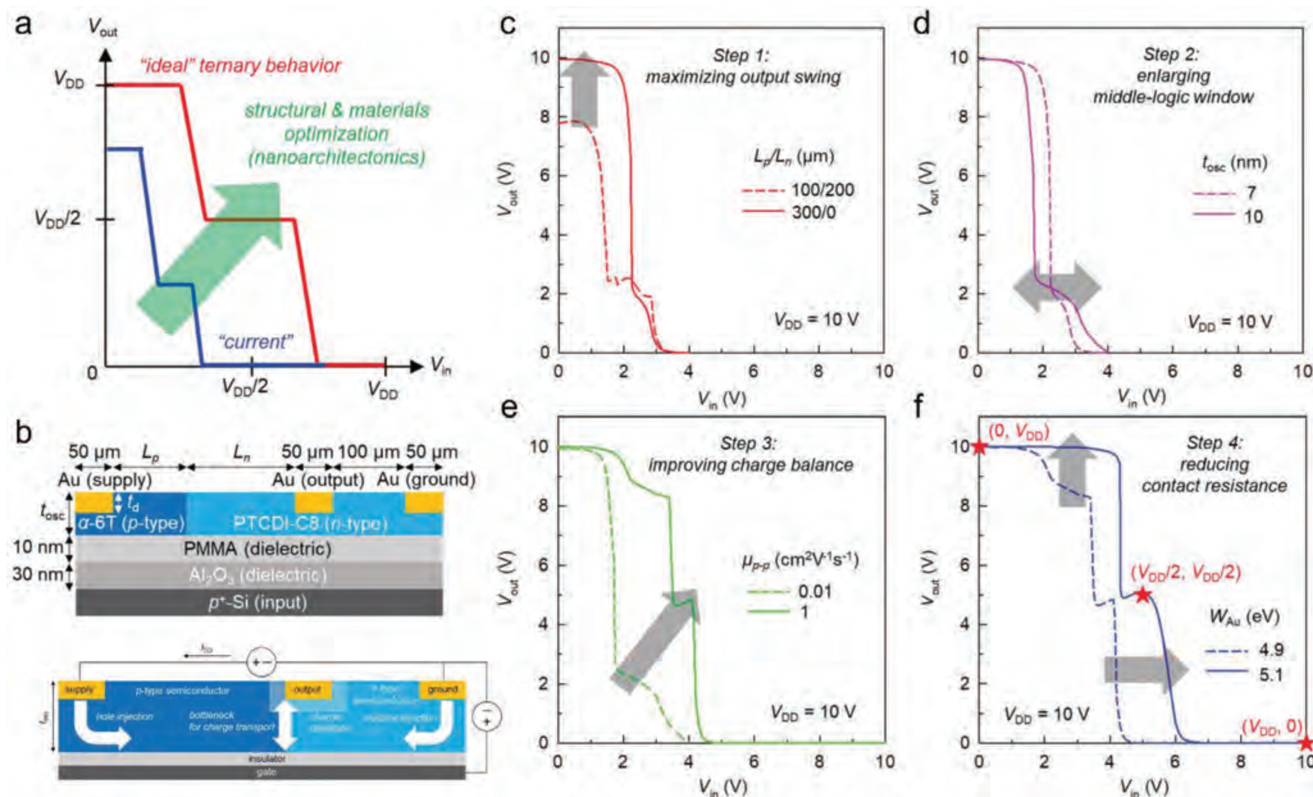

Figure 23. Device modeling of ternary inverters. a) Conceptual illustration for achieving ideal VTC characteristics.[38] b) Cross-sectional illustration of the 6T/PTCDI-C8 heterojunction-based ternary inverter. Input-output characteristics with different c) channel lengths, d) semiconductor thicknesses, e) carrier mobilities, and f) contact barriers. a–f) Reproduced with permission.[38] Copyright 2021, Royal Society of Chemistry.

characterizations and DFT calculations, it was determined that the room-temperature NDT performance arises from the synergistic effects of trap-assisted tunneling and gate-tunable nonlinear band shifts. More importantly, the feasibility of constructing a quaternary inverter using a double-peak NDT device was confirmed through a Cadence circuit simulation (Figure 24c).[15] These quaternary inverters based on double-peak NDT devices provide guidelines for future MVL computing.

Given the ultrathin nature of 2D materials, dielectric engineering could significantly alter their electrical properties and device performance.[108] In 2020, dielectric engineering on stepped h-BN gate dielectric was employed to increase the number of NDT peaks of anti-ambipolar WSe_2 transistors.[103] In simulations, these multiple-peak NDT devices could enable ternary, quaternary, and even quinary inverters, which shows a direct way to increase the radix of MVL circuits. In comparison to traditional MVL systems relying on complex heterojunction channels, the dielectric engineering concept with a stepped gate dielectric offers effective simplification of the device structure and reduction in interconnects.

Surface functionalization is an alternative approach to introducing NDT regions in AATs devices. This method is regarded as an effective and nondestructive technique for low-dimensional materials. In 2021, Son et al. reported that partial coverage of cross-linked PMMA (electron donor) could modify the electrical characteristics of the ambipolar $MoTe_2$ channel in $MoTe_2/MoS_2$ heterojunction.[228] As a result, this cross-linked PMMA surface modification led to the realization of quaternary inverter operations with four distinct logic states. It is worth noting that surface functionalization does not introduce lattice disorders or material degradation into semiconducting materials.[225] Instead, it provides a simple and nondestructive approach to tuning the electrical properties of semiconducting materials for utilization in MVL circuits.

5.2.2. Organic Material-Based Quaternary Inverters

Organic semiconductors are good candidates for building quaternary inverters because of their tunable molecular properties and feasible deposition in large areas. In early 2023, Panigrahi et al. developed an organic quaternary inverter based on two anti-ambipolar heterojunctions of p-C8-BTBT/n-PTCDI-C8 and p-C8-BTBT/n-PhC2-BQQDI (Figure 24d).[14] In this case, both the PTCDI-C8 and PhC2-BQQDI layers form p-n heterojunctions with the C8-BTBT layer, creating double vertically stacked heterojunctions around the center of the AAT channel. Together with the continuous C8-BTBT top layer, three conducting paths are formed in this organic heterojunction AAT, resulting in double NDT characteristics during gate voltage sweeping (Figure 24e). Notably, an organic quaternary logic circuit was successfully fabricated by connecting the double-peaked AAT with an n-type transistor, allowing for the equiprobable accessibility to the four logic states ("0", "1/3", "2/3", and "1") (Figure 24f).

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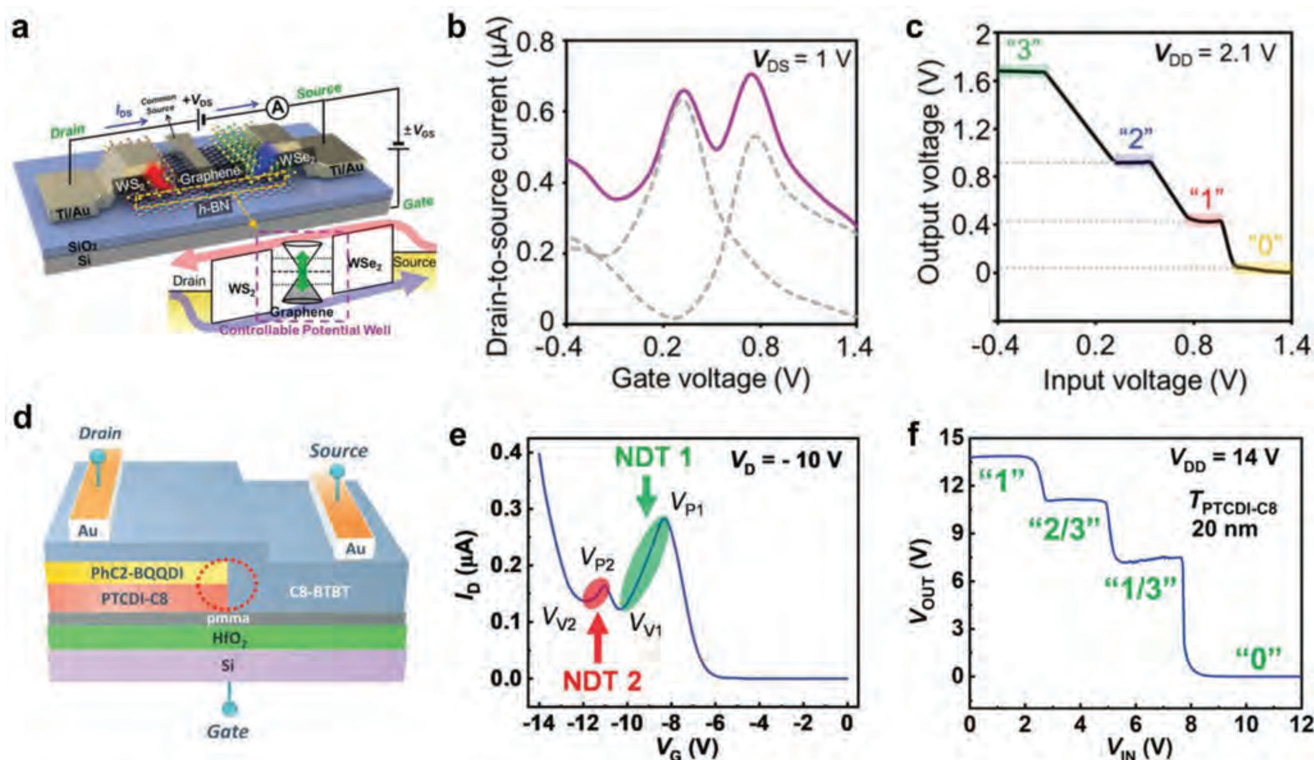

Figure 24. 2D-based and organic-based quaternary inverters. a) Schematic diagram and b) transfer characteristics of the double-peak WS_2-graphene-WSe_2 heterojunction device.[15] c) VTC curve of quaternary inverter based on a WS_2-graphene-WSe_2 device. d) Schematic illustration of a double-peaked organic AAT comprising two stacked p-n heterojunctions.[14] e) Transfer curve and NDT characteristics of the double-peaked organic AAT. f) VTC characteristics of the organic quaternary inverter with four logic states. a–c) Reproduced with permission.[15] Copyright 2019, Wiley-VCH. d-f) Reproduced with permission.[14] Copyright 2023, Wiley-VCH.

5.2.3. External Field-Induced Quaternary Inverters

In 2017, light-induced M-shaped anti-ambipolar behavior was found in vertically stacked p-WSe_2/n-SnS_2 vdW heterojunctions fabricated using the PMMA-assisted transfer method.[70] A standard Λ-shaped transfer curve was achieved under dark conditions with a high PVR of ≈10^5, while the light illumination would induce the M-shaped anti-ambipolar behavior of p-WSe_2/n-SnS_2 vdW heterojunctions. The tunable Schottky barrier between the channel and the Au electrodes contributed to the added “on” state.

In 2021, double-peak AATs were demonstrated by integrating InSe/WSe_2 heterojunction on flexible polyethylene terephthalate (PET) substrates (**Figure** 25a).[72] Strain-dependent characterizations confirm the presence of two conduction pathways at the heterojunction (Figure 25b,c). Usually, carrier transport passes through the lateral junction edge, while applying mechanical strain can allow an alternative conduction path via the vertical injection. With proper adjustment of the two transport contributions at 1.65% strain, M-shaped anti-ambipolar behavior with similar peak currents and PVR of ≈10^2–10^3 could be realized (Figure 25d).[72] More importantly, the obtained double-peak AATs could be employed in building a quaternary inverter, as shown in the VTC curve in Figure 25e. The fewer interconnects, and fewer transistors lead to the reduced power consumption down to 0.9 μW, which is lower than traditional CMOS-based MVL systems.[229]

Unlike conventional material-based MVL devices with large active regions, nanoscale low-dimensional MVL devices feature significantly shrinking device dimensionality. The downscaling active region can reduce the junction capacitance and thus make the devices intrinsically faster and more energy efficient. More importantly, due to their unique structures, the impact of external field effects, such as electric field, light field, and strain effect, usually become pronounced, bringing unexpected electrical behaviors for functional devices.

5.3. Logic Gates and Circuits

Logic gates are fundamental components of digital circuits that make decisions based on a combination of digital signals from their inputs. There are seven fundamental binary logic gates in Boolean algebra: AND, OR, XOR, NOT, NAND, NOR, and XNOR. Among them, the NOT gate has only one input, acting as a logical inverter to reverse the logic state, while the other two-input logic operation relationships are defined by the truth tables shown in **Table** 4.

5.3.1. Reconfigurable Basic Logic Gates

Reconfigurable logic circuits would benefit the high-throughput data processing, reduce power consumption, and facilitate

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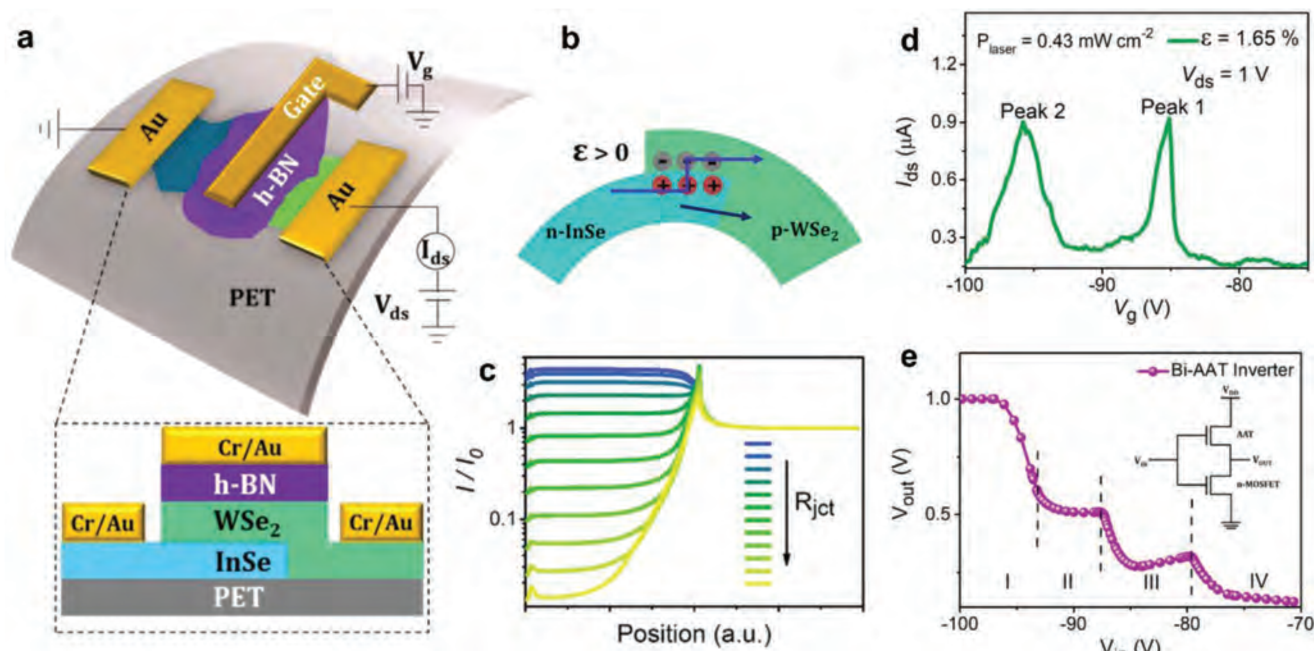

Figure 25. External field-induced quaternary inverters. a) Schematic illustration of InSe/WSe_2 AATs on a flexible substrate.[72] b) Schematic illustration of two carrier pathways in the InSe/WSe_2 heterojunction under strain. c) The current distribution along the nSe/WSe_2 heterojunction direction as a function of junction resistance values. d) Transfer curve of double-peak AAT with a maximum applied 1.65% strain. e) Quaternary inverter based on bi-anti-ambipolar transistor showing four distinct logic levels. a–e) Reproduced with permission.[72] Copyright 2021, American Chemical Society.

large-scale integration. In 2022, reconfigurable MVL circuits were built on organic α–6T/PTCDI-C8 heterojunction AATs (**Figure 26a–c**).[32] With a dual-gate structure, i.e., the bottom-gate (V_{IN1}) and top-gate (V_{IN2}), five basic logic operations were demonstrated, including AND, OR, NAND, NOR, and XOR (Figure 26d). Thus far, multiple logic operations have also been achieved by single-electron transistors based on Coulomb oscillation at cryogenic temperatures down to 40 K.[230–232] In contrast, the dual-gate organic heterojunction AATs enable room-temperature multiple logic gate operations. Furthermore, a reversible switch between two logic functions (NAND/NOR and OR/XOR) can be achieved by varying the drain voltage. In the traditional CMOS architecture, four and twelve transistors are needed to conduct NAND and XOR functions, respectively,[233–235] while the reconfigurable multiple logic gate operations in this work rely solely on single dual-gate organic AATs.

In 2023, a dual-gate AATs with a 2d ReS_2/WSe_2 heterojunction was developed to realize reconfigurable logic operations.[69] By controlling the input voltages, the characteristic of dual-gate vdW heterojunction AATs can be effectively controlled, with the generated drain current serving as the output signal. This enables all the two-input basic logic operations, including AND, OR, XOR, NAND, NOR, and XNOR. Apart from the five basic logic gates already demonstrated in dual-gate organic heterojunctions,[32] the additional XNOR gate operation was realized in ReS_2/WSe_2 heterojunction by leveraging the N-shaped transfer curves of AATs. These works demonstrate the feasibility of building multifunctional and multivalued logic circuits using a single transistor, presenting a promising approach to simplify logic circuits and increase integration density.

Table 4. Truth table of basic binary logic gates.

INPUTS		OUTPUTS					
IN1	IN2	AND	NAND	OR	NOR	XOR	XNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

5.3.2. NMAX and NMIN Logic Gates

To demonstrate the applicability of MVL circuits for complex logic operations, negated MAX (NMAX) and negated MIN (NMIN) logic gates were also built based on MoS_2/chemically treated MoS_2 channel and PEDOT: PSS/P3HT channel with resistive-loads.[10,236] The MIN gate in ternary logic corresponds to the AND gate in binary logic, while the MAX gate corresponds to the OR gate.[237] Consequently, the NMIN and NMAX gates can be readily implemented by replacing the binary CMOS with the proposed NDT devices in NAND and NOR gates. As shown in the truth table in **Table 5**, in R-valued logic, the outputs of NMIN and NMAX functions correspond to the remainder of MAX and MIN functions. The performance of the proposed NMIN and NMAX logic gates was verified by their temporal responses under the application of two input voltages, by which stable ternary logic states and ideal output voltage swings are obtained.[10,236] The ultrashort

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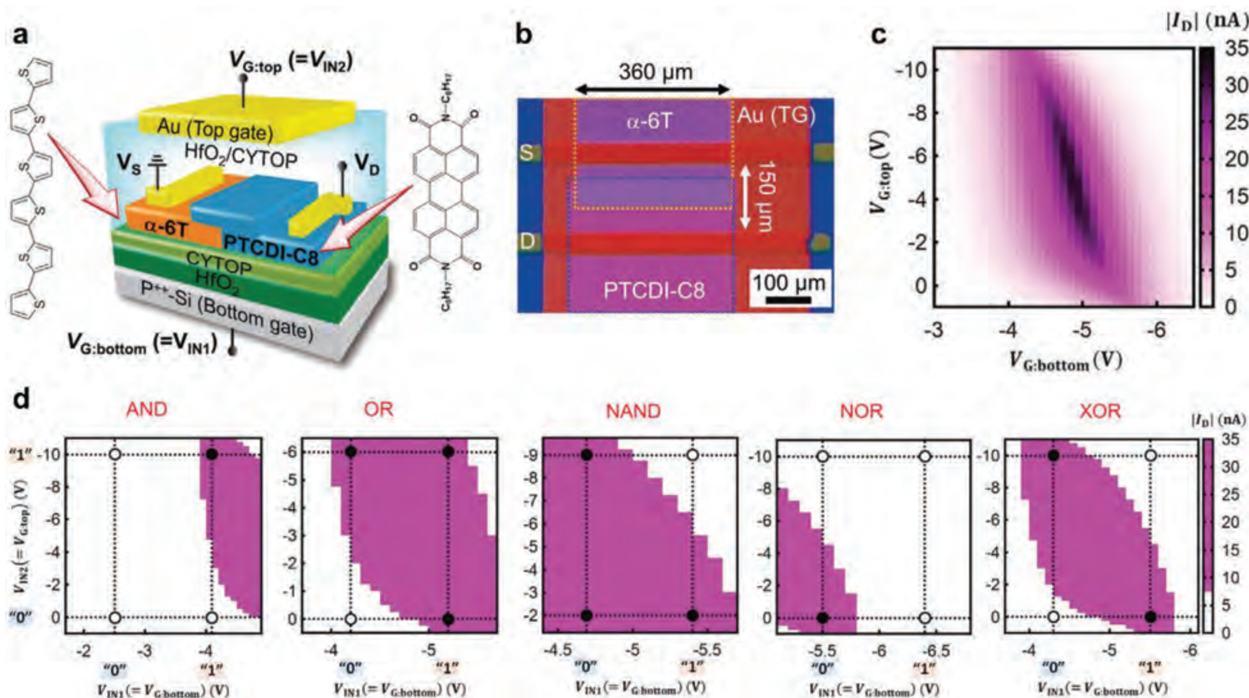

Figure 26. Logic gates based on anti-ambipolar heterojunctions. a) Device structure, b) optical image, and c) 2D input-output mappings of the dual-gate organic α−6T and PTCDI-C8 heterojunction AATs.[32] d) Two-input AND, OR, NAND, NOR, and XOR logic gate operations of the dual-gate organic AATs. a-d) Reproduced with permission.[32] Copyright 2022, Wiley-VCH.

vertical organic PEDOT: PSS/P3HT heterojunction channel allows a potential high accessing frequency over 10 MHz and a full voltage swing within 1 V.[236] Further optimization of the device structure and interface property could further improve the performance of these circuits.[238]

5.3.3. Ternary Full-Adder Circuits

Most recently, 10 novel logic gates, including TAND, TOR, NCONS, NANY, SUM, and a balanced ternary full-adder, were designed based on the inkjet-printable AATs and CNT PMOSs.[96] In particular, three logic input states (−1, 0, +1) were employed to realize these ternary logic operations, as presented in the truth table in **Table 6**. With a compact design, the printed ternary full-adder could be built only using a minimum number of 58 transistors, comprising 41 CNT PMOSs and 17 AATs. Compared to the full-adder design utilizing BP ambipolar FETs (99 transistors),[239] CNTFET (74 transistors),[240] and memristor (97 transistors),[241] 22.6% of component transistors would be reduced in such printed AATs-based ternary full-adder circuits.

Table 5. Truth table of NMIN (NMAX) logic gates.

NMIN (NMAX)	0	1	2
0	2 (2)	2 (1)	2 (0)
1	2 (1)	1 (1)	1 (0)
2	2 (0)	1 (0)	0 (0)

These results will benefit the convenient manufacturing of future ternary systems as well as wearable consumer electronics.[96]

5.4. Neural Networks and Circuits

Thanks to the dynamic changes in synaptic connection strength, both simulated artificial neural networks and hardware spiking neuron circuits can be made to process data and identify patterns with improved robustness, plasticity, and fault tolerance. Anti-ambipolar heterojunctions and their devices possess advantageous anti-ambipolar characteristics and high tunability, making them highly suitable for various neuromorphic computing applications.

Table 6. Truth table of TAND, TOR, NCONS, NANY, and SUM logic gates.

INPUTS		OUTPUTS				
IN1	IN2	TAND	TOR	NCONS	NANY	SUM
−1	−1	−1	−1	+1	+1	+1
−1	0	−1	0	0	+1	−1
−1	+1	−1	+1	0	0	0
0	−1	−1	0	0	+1	−1
0	0	0	0	0	0	0
0	+1	0	+1	0	−1	+1
+1	−1	−1	+1	0	0	0
+1	0	0	+1	0	−1	+1
+1	+1	+1	+1	−1	−1	−1

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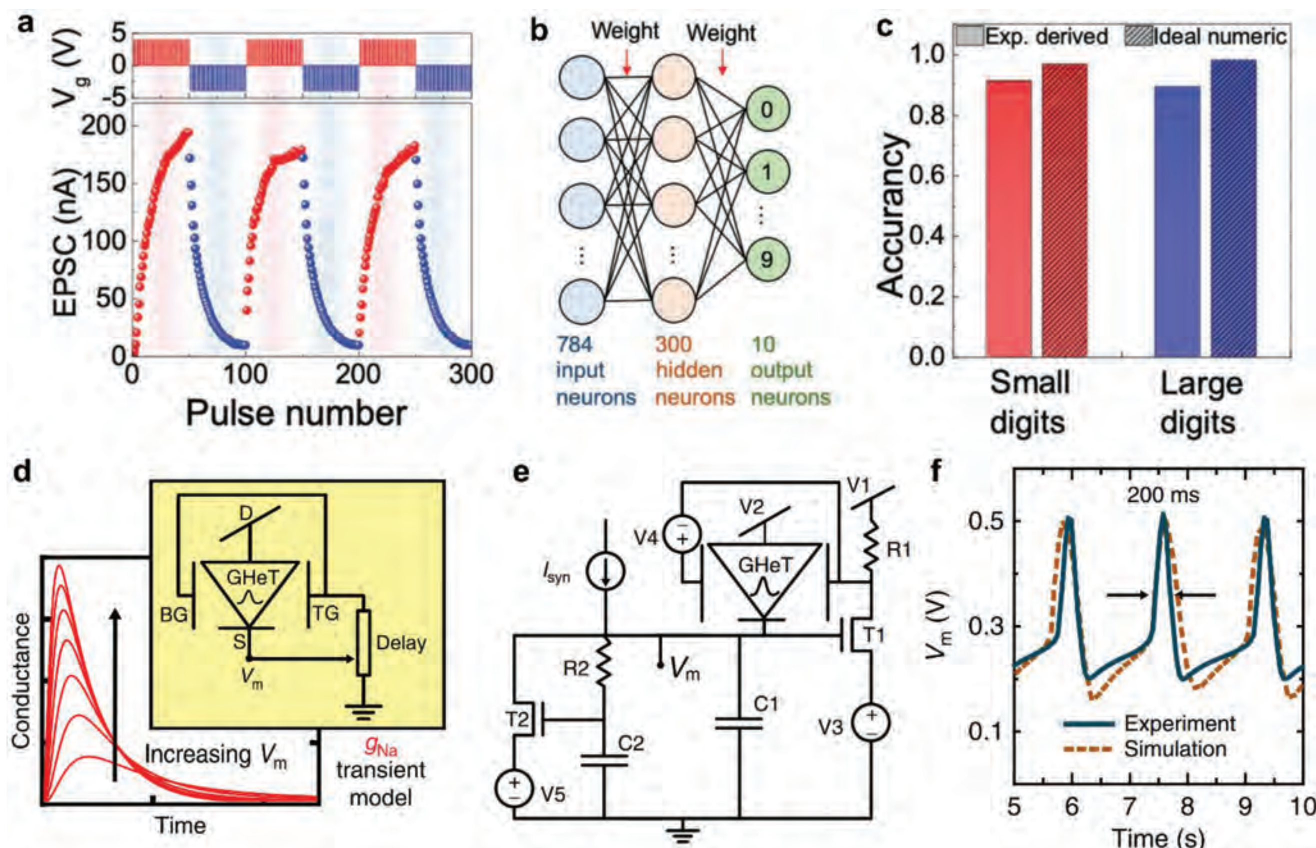

Figure 27. Neural networks and circuits. a) Long-term potentiation/depression processes of the BP/ReS_2 heterojunction synaptic device.[67] b) Schematics of a three-layer neural network and (c) their recognition accuracy for small and large handwritten digit images. d) Mimicked transient behavior of Na^+ conductance in anti-ambipolar SWCNTs/MoS_2 Gaussian heterojunction transistors.[92] e) Full circuit diagram of hardware spiking neuron circuits and f) their experimental spiking/resetting behavior. a–c) Reproduced with permission.[67] Copyright 2020, Wiley-VCH. d,e) Reproduced with permission.[92] Copyright 2020, Springer Nature.

5.4.1. Artificial Neural Networks

Taking inspiration from the neuronal organization in biological neural networks, artificial neural networks hold the potential to perform brain-like cognitive tasks. With the anti-ambipolar characteristics and unique trilingual synaptic tunability, the artificial electronic synapse based on the BP/ReS_2 heterojunction showed repeatable excitatory and inhibitory states by alternating 50 potentiations and depressions presynaptic input (**Figure** 27a).[67] Exploiting the long-term plasticity characteristics of the BP/ReS_2 heterojunction, a three-layer artificial neural network comprising 784 input neurons, 300 hidden neurons, and 10 output neurons was designed and utilized for handwritten image recognition (Figure 27b). Clearly, the synaptic weights could be more efficiently updated via parallel processing when compared to the CMOS architecture. As a result, recognition accuracy ratios of 91.3% and 89.5% were achieved for small and large handwritten digit images, respectively, after 40 epochs (Figure 27c). Moving forward, the recognition accuracy could be further improved by achieving a linear and symmetrical conductance change in long-term potentiation/depression processes.

5.4.2. Spiking Neuron Circuits

Tunable Gaussian functions are important in hardware-level neuromorphic implementations and artificial learning paradigms. However, using analog CMOS circuits to mimic Gaussian response usually suffer from limited programmability and high bias current.[242] To fulfill this aim, in 2020, an advanced dual-gated Gaussian transistor was built on anti-ambipolar SWCNTs/MoS_2 heterojunction for utilization in spiking neuron implementation.[92] The dual-gated architecture could generate the fully tunable Gaussian anti-ambipolar response in a single heterojunction device, which could emulate the transient behavior of Na^+ conductance (Figure 27d). According to Choi et al., neural networks comprising Gaussian synapses demonstrate better convergence properties when compared to neural networks with linear-multiplying synapses.[243,244]

Figure 27e,f depicts the integrated spiking neuron circuits based on Gaussian transistors, demonstrating stable spiking and resetting behaviors while consuming ≈250 nJ of energy per spike.[92] By emulating biological ion channels in neurons, the artificial neurons built using these dual-gated Gaussian devices

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exhibit a plethora of advanced spiking response functions, including phasic spiking, delayed spiking, and tonic bursting. These findings highlight the substantial potential of AATs-based spiking neuron circuits in facilitating future low-power neuromorphic computing, computer vision, and natural language processing applications.

6. Conclusion and Outlook

This review has provided a comprehensive overview of the historical and recent advances in anti-ambipolar heterojunctions, highlighting their significance as a driving force in materials, devices, circuits, and broad research.

The anti-ambipolar heterojunction, characterized by a gate-tunable Λ-shape transfer characteristic, allows for positive and negative transconductance within a single device. For adaptability in various logic circuit applications, it is essential to dynamically adjust the transport characteristics of anti-ambipolar heterojunctions. Therefore, different influencing factors and geometric optimizations have been considered to improve the device performance, as discussed in the Fundamentals section (Section 2). At the same time, theoretical predictions have also served as valuable tools in offering guidance for enhancing device performance.

The development of materials science has been the primary catalyst for technological advancements in the semiconductor industry over the past few decades. Integrating constituent semiconductor materials is vital to fabricate high-performance anti-ambipolar devices for achieving the desired transfer characteristics. So far, significant efforts have been devoted to preparing and utilizing new semiconductor nanomaterials, leading to a substantial accumulation of experience in the field of anti-ambipolar heterojunctions. The construction of anti-ambipolar heterojunctions has been realized on a range of semiconducting materials, such as 2D, 1D, organic, and inorganic materials, as detailed in the Materials section (Section 3).

The above results demonstrate that the transport characteristics of AATs devices can be dynamically designed and adjusted for specific device functions. On the one hand, achieving a balanced carrier concentration on both the p- and n-sides can be accomplished through energy structure engineering or doping processes. On the other hand, using the different capacitance of the insulating layer would effectively modulate the range of the on-state gate voltage to ensure low energy consumption. These results enable flexibility and adaptability in various functional device applications, including photodetection, frequency modulation, and logic-in-memory, which can be seen in the Devices section (Section 4).

Driven by device miniaturization, FETs have emerged as the fundamental building blocks of information technology.[109,245] However, it is currently challenging to continue shrinking the size of transistors, limited by the nano-fabrication precision and short-channel effects.[246,247] This also calls for an alternative technology to settle the encountered bottleneck problem roundaboutly. Due to the characteristics of multivalued logic states with more than three different logic states, the advent of AATs-based MVL circuits promises to reduce the transistor density in logic circuits without sacrificing circuit performance. The recent results about AATs-based MVL circuits, including ternary inverters, quaternary inverters, basic logic gates, and reconfigurable MVL circuits, have been detailly discussed in the Circuits section (Section 5).[8,10]

Currently, the research on anti-ambipolar heterojunctions is in the exploratory stage. Given the extensive unexplored engineering possibilities, a significant research focus is expected to explore anti-ambipolar mechanisms, material combinations, device concepts, and circuit systems. Future research endeavors are expected to uncover new phenomena and applications that can fully maximize the unique capabilities of anti-ambipolar heterojunctions, thereby providing exciting possibilities for further advancements. In these circumstances, four important questions need to be addressed to develop advanced anti-ambipolar devices and circuits:

i. What are the universal material synthesis methods and compatible device fabrication schemes of the AATs devices? For instance, when considering 2D materials, mechanical exfoliation provides a convenient method to screen and identify suitable active 2D channels for anti-ambipolar applications. However, mechanical exfoliation has limitations in terms of production yield and morphology control (e.g., thickness, size, and shape), which, in turn, restrict the large-area practical applications of 2D materials. To develop high-performance AATs and multivalued logic gates, versatile material synthesis methods, including physical vapor deposition, chemical vapor deposition, and solution depositions, should be explored to solve the cost-effectiveness issue of practical utilizations. The diversification of junction formation will remain critical in advancing the field. Exploring similar or alternative junction designs and fabrication techniques will uncover new phenomena and enable the development of practical applications in various domains.

ii. What are the suitable p-channel and n-channel materials with proper band alignment for efficient anti-ambipolar devices? Benefiting from the ultimate size downscaling and naturally terminated surfaces, those low-dimensional 2D/2D or 1D/2D vdW heterostructures may show better frequency characteristics, lower energy dissipation, and better carrier concentration modulation than conventional multivalued logic devices. Besides, as most organic semiconductor materials are p-type and inorganic semiconductor materials are n-type, anti-ambipolar heterojunctions made by hybrid materials would be a good choice.

iii. What are the fundamental operation mechanisms of these anti-ambipolar devices? In other words, what are the design guidelines to improve the performance and reliability of the devices? While the observed electrical characteristics may be similar, the operation mechanism depends on the specific constituent materials and device configurations. The precise carrier transport mechanism underlying these devices remains unclear. Therefore, it is necessary to conduct systematic experiments in conjunction with physical modeling to gather additional information and establish guidelines for device design. A clear understanding of the operating mechanisms will facilitate device optimization with respect to component materials, geometrical considerations, interface engineering, and fabrication techniques.

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iv. What technical specifications should anti-ambipolar heterojunctions meet to compete with or complement existing silicon-based CMOS technologies? In the short term, it is more realistic to partially integrate AATs-based MVL modules with mature binary silicon-based CMOS technologies on the same chip. In this early stage, individual AATs require high peak-to-valley ratios, high peak currents, and a narrow on-state bias range, whereas the constructed AATs-based MVL modules need balanced voltage levels, large noise margins, low operating voltage, and a full output swing. In the mid- and long-term perspectives, the MVL technology possesses the sufficient potential to approach and eventually compete with conventional binary technologies. With this objective in mind, anti-ambipolar heterojunctions need to assess their feasibility concerning energy consumption, environmental stability, scalability, reliability, and compatibility.
v. How do these anti-ambipolar devices be effectively integrated into large-area complex MVL circuits to perform beyond von Neumann computing task? We should aim to assess the performance limits and operation mechanisms of the MVL devices/circuits to establish relevant design guidelines. Also, these findings would provide feedback to select suitable materials as device channels and further optimize the device dimensions, reliability, and fabrication processes. Furthermore, multifunctionality can provide an additional advantage in enhancing the physical integration capacity, significantly reducing the number of transistors required in an integrated system.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

anti-ambipolar transistors, heterojunctions, homojunctions, multivalued logic circuits, negative differential transconductance

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