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Electronic/Optoelectronic Memory Device Enabled by Tellurium-based 2D van der Waals Heterostructure for in-Sensor Reservoir Computing at the Optical Communication Band

Jiajia Zha, Shuhui Shi, Apoorva Chaturvedi, Haoxin Huang, Peng Yang, Yao Yao, Siyuan Li, Yunpeng Xia, Zhuomin Zhang, Wei Wang, Huide Wang, Shaocong Wang, Zhen Yuan, Zhengbao Yang, Qiyuan He, Huiling Tai, Edwin Hang Tong Teo, Hongyu Yu, Johnny C. Ho, Zhongrui Wang, Hua Zhang,* and Chaoliang Tan**

Although 2D materials are widely explored for data storage and neuromorphic computing, the construction of 2D material-based memory devices with optoelectronic responsivity in the short-wave infrared (SWIR) region for in-sensor reservoir computing (RC) at the optical communication band still remains a big challenge. In this work, an electronic/optoelectronic memory device enabled by tellurium-based 2D van der Waals (vdW) heterostructure is reported, where the ferroelectric $CuInP_2S_6$ and tellurium channel endow this device with both the long-term potentiation/depression by voltage pulses and short-term potentiation by 1550 nm laser pulses (a typical wavelength in the conventional fiber optical communication band). Leveraging the rich dynamics, a fully memristive in-sensor RC system that can simultaneously sense, decode, and learn messages transmitted by optical fibers is demonstrated. The reported 2D vdW heterostructure-based memory featuring both the long-term and short-term memory behaviors using electrical and optical pulses in SWIR region has not only complemented the wide spectrum of applications of 2D materials family in electronics/optoelectronics but also paves the way for future smart signal processing systems at the edge.

1. Introduction

Emerging 2D materials provide a new dimension to advance electronics/optoelectronics.[1–4] This is particularly important in this era of Internet of things (IoT) and big data, where the computing complexity undergoes a geometric progression at the edge sensory nodes and poses a huge challenge to traditional Si-based devices.[5–8] The in-sensor reservoir computing (RC) based on 2D materials provides a promising software-hardware codesign to address this challenge.[9] RC features intrinsic advantages for edge learning[10] since only the lightweight readout layer needs to be optimized, that leads to a significant reduction of training complexity.[11–13] In 2021, Sun et al. demonstrated an in-sensor RC system based on 2D SnS for language learning.[14] Liu et al.

J. Zha, W. Wang, Q. He, J. C. Ho
Department of Materials Science and Engineering
City University of Hong Kong
Hong Kong 999077, P. R. China

J. Zha, H. Huang, P. Yang, Y. Xia, H. Wang, C. Tan
Department of Electrical Engineering
City University of Hong Kong
Hong Kong 999077, P. R. China
E-mail: chaoltan@cityu.edu.hk

S. Shi, S. Wang, Z. Wang
Department of Electrical and Electronic Engineering
University of Hong Kong
Hong Kong 999077, P. R. China
E-mail: zrwang@eee.hku.hk

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S. Shi, H. Yu
School of Microelectronics
Southern University of Science and Technology
Shenzhen, Guangdong 518055, P. R. China

A. Chaturvedi, E. H. T. Teo
School of Materials Science and Engineering
Nanyang Technological University
50 Nanyang Ave, Singapore 639798, Singapore

Y. Yao, S. Li, H. Zhang, C. Tan
Department of Chemistry
City University of Hong Kong
Hong Kong 999077, P. R. China
E-mail: Hua.Zhang@cityu.edu.hk

Z. Zhang, Z. Yang
Department of Mechanical Engineering
City University of Hong Kong
Hong Kong 999077, P. R. China

reported a multimode and multiscale RC based on 2D α-In_2Se_3 in 2022 for digit and quick response (QR) code recognition.[15] But limited by the bandgap of the chosen materials, the photoresponse of these systems was in the visible light region. Although there are many 2D material-based memory devices developed in the past decade,[16–27] most of them can only respond to electrical signals. For a few optoelectronic memory devices, the wavelength is restricted to the ultraviolet to visible (UV–vis) region. The single electrical responsivity reported on most devices may defeat the advantage of in-sensor computing in terms of efficiency and circuit-complexity for the redundant integration with optoelectronic circuits. On the other hand, infrared (IR) light is of particular importance in optical communication, night vision, and thermography,[28,29] the memory unit with the ability of sensing IR signal will no doubt broaden its prospects.

Among promising options provided by 2D family, tellurium (Te) is a van der Waals (vdW) semiconductor with truly one-dimensional (1D) crystal structure, where single helical molecular chains are stacked together via vdW intercalation.[30,31] Te has long been pursued but until recently been rediscovered as a charming vdW material for electronics and optoelectronics.[32] The naturally terminated surfaces except for the two ends endow Te with advantages over conventional three-dimensional (3D) materials, the latter often suffers from surface-induced performance degradation.[30] Te is a *p*-type semiconductor with thickness-dependent bandgap (≈1.04 eV for monolayer and 0.35 eV for bulk), which covers the short-wave infrared (SWIR) region. In addition, Te has a high field-effect hole mobility up to 1370 $cm^2\ V^{-1}\ s^{-1}$ at room temperature.[32,33] In virtue of these admiring electronic properties, Te has been widely used in building high-performance field-effect transistors (FETs), *p*-type metal-oxide-semiconductor (*p*-MOS) inverters, and 3D monolithic circuits.[32–34] Te has also been employed in high-performance nanoscale memristors.[35,36] More importantly, as a narrow bandgap semiconductor with air stability, it is also promising for fabrication of SWIR photodetectors with superior performance,[37–41] thus holding a great promise for in-sensor RC systems at the optical communication band (1260–1675 nm).

Z. Yuan, H. Tai
State Key Laboratory of Electronic Thin Films and Integrated Devices
School of Optoelectronic Science and Engineering
University of Electronic Science and Technology of China (UESTC)
Chengdu 610054, P. R. China

Z. Yang
Department of Mechanical and Aerospace Engineering
Hong Kong University of Science and Technology
Hong Kong 999077, P. R. China

E. H. T. Teo
School of Electrical and Electronics Engineering
Nanyang Technological University
Singapore 639798, Singapore

H. Zhang
Hong Kong Branch of National Precious Metals Material Engineering
Research Center (NPMM)
City University of Hong Kong
Hong Kong, P. R. China

H. Zhang, C. Tan
Shenzhen Research Institute
City University of Hong Kong
Shenzhen 518057, P. R. China

In this work, we report an electronic/optoelectronic dual-responsive memory device enabled by Te-based vdW heterostructure, in which the Te nanoflake serves as the channel material and the 2D ferroelectric $CuInP_2S_6$ (CIPS) functions as the dielectric layer. This device exhibits long-term potentiation/depression (LTP/LTD) via electrical stimuli and short-term potentiation (STP) triggered by SWIR laser pulses. The manifestation of different memory behaviors driven by electrical and optical signals enable a fully memristive in-sensor RC system at the optical communication band (represented by 1500-nm optical signal), which combines the role of transducers, message decoders and artificial intelligence (AI) accelerators in smart edge signal processing. This is revealed by its capability to learn the classification of the representative Modified National Institute of Standards and Technology (MNIST) handwritten images transmitted through optical fibers, achieving an accuracy ≈0.8 that is comparable to the software baseline.

2. Results and Discussion

2.1. Fabrication and Characterization of the MFMIS Device

The electronic/optoelectronic dual-responsive memory device has a metal-ferroelectric-insulator-semiconductor (MFMIS) architecture. **Figure 1**a shows the scheme of our vdW heterostructure on a prepatterned metal bottom gate (M: Metal), which is in the FET-like geometry. From the bottom up, the different layers are CIPS (F: Ferroelectric), graphene (M: Metal), h-BN (I: Insulator), and Te nanoflake (S: Semiconductor), respectively. Among the vdW heterostructure, CIPS is a room-temperature 2D ferroelectric crystal. The reported transition temperature of CIPS is ≈320 K and the switchable polarization remains observable when its thickness is reduced to ≈4 nm.[42] After applying electrical stimuli, the induced polarization in the ferroelectric CIPS nanoflake will help maintain the conductance of the Te channel.[43] The graphene (Gr) nanoflake on the CIPS nanoflake is crucial in compensating both downward and upward polarizations in CIPS,[43–45] and works as the gate electrode in the internal Gr/h-BN/Te FET. The h-BN nanoflake between the Te and graphene nanoflakes serves as the insulating dielectric layer. The optical microscope image of a typical MFMIS memory device is shown in Figure 1b and different nanoflakes are indicated by dashed curves in different colors. In this heterostructure, the mechanically exfoliated CIPS, graphene, and h-BN nanoflakes are in the thickness of 161.0 nm, 13.9 nm, and 26.0 nm, respectively, which is shown in Figure 1c. The top Te nanoflake with a thickness of 22.9 nm was synthesized by a hydrothermal method.[32,37] The height profiles of these materials were acquired by the atomic force microscope (AFM) as shown in Figure S1 (see Supporting Information). The fabrication process of our device is illustrated in Figure S2 (Supporting Information). On the top of the prepatterned chromium/gold (Cr/Au: 5/100 nm) bottom gate, we stacked these 2D nanoflakes step by step through a wet transfer method.[46] The source/drain/internal gate electrodes were defined by the standard electron beam lithography (EBL) followed by the thermal evaporation of Au (70 nm). Figure 1d shows the Raman spectra of these vdW materials. For the exfoliated

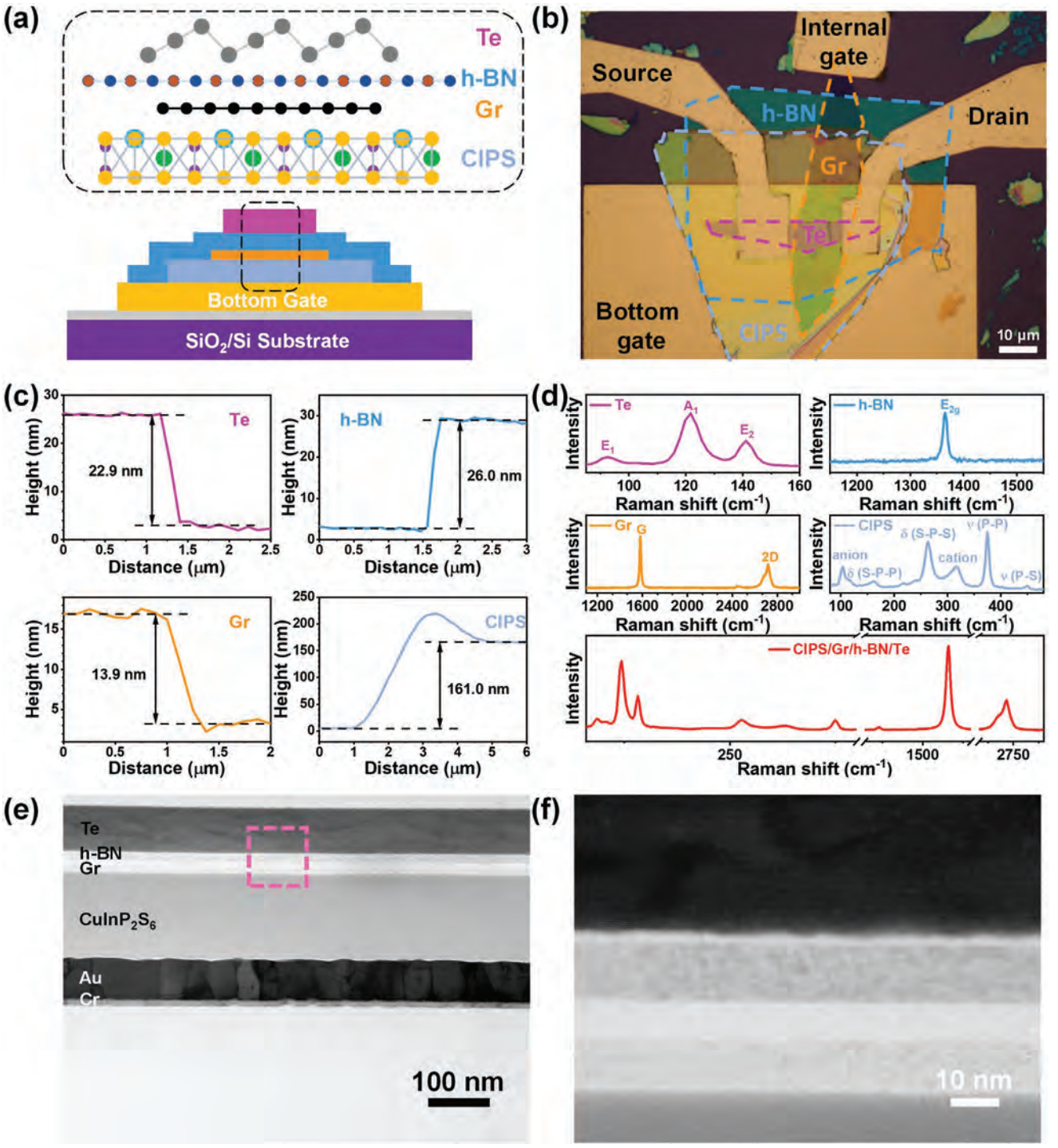

Figure 1. Te-based MFMIS device. a) Schematic illustration of the MFMIS device, where Te nanoflake serves as the channel material, and the insulating h-BN layer places between Te nanoflake and Gr layer, which is on the top of the ferroelectric dielectric layer CIPS. At the bottom of the vdW heterostructure, Au is used as the bottom gate. b) Optical microscope image of a typical MFMIS device. Different materials are indicated by dashed curves with different colors. Scale bar, 10 μm. c) Height profiles of the materials in the heterostructure in (b) measured by AFM. d) Raman spectra of Te, h-BN, Gr, CIPS, and CIPS/Gr/h-BN/Te heterostructure. e) HRTEM image of the cross section in the fabricated MFMIS device. f) STEM image of the area indicated by the pink dashed box in (e).

CIPS nanoflake, there are six active modes (102.2 cm^{-1} for the anion, 161.8 cm^{-1} for δ (S-P-P), 263.5 cm^{-1} for δ (S-P-S), 316.4 cm^{-1} for the cation, 374.2 cm^{-1} for ν (P-P), and 449.1 cm^{-1} for ν (P-S)), consistent with previous reports on thick CIPS nanoflakes.[47,48] In terms of the graphene nanoflake, its high quality is evidenced by the lack of *D* peak in its Raman

spectra. Besides, the intensity of *G* peak is much higher than that of *2D* peak, which suggests the multilayer nature of the graphene flake.[49] In addition, both the h-BN and Te nanoflakes in this heterostructure exhibit similar Raman spectra to previous reports.[32,50] To further confirm the structure of the MFMIS device and demonstrate the clean interface between these 2D materials, we further conduct the high-resolution transmission electron microscopy (HRTEM) and scanning transmission electron microscopy (STEM) characterizations on the cross-section of the fabricated heterostructure, which are shown in Figure 1e,f. Both the HRTEM and STEM images demonstrate that our fabricated vdW heterostructure has clean interfaces between these 2D materials even though the stack process is a little bit complicated. Moreover, the corresponding energy-dispersive spectrometry (EDS) mapping also show the homogenous distribution of elemental compositions of these 2D materials within the heterostructure, further confirming the chemical composition of the 2D vdW heterostructure (Figure S3, Supporting Information).

The ferroelectric property of the exfoliated CIPS flake was characterized by a piezoresponse force microscope (PFM), as shown in Figure S4 (Supporting Information). Figure S4a (Supporting Information) is the optical microscope image of the measured CIPS sample, which was deposited onto a conducting substrate and exfoliated from the same maternal crystal with those nanoflakes used in fabricating the heterostructures. The inset shows the AFM image of the region indicated by the red dashed box. The thickness measured along the green dashed line in the inset of Figure S4a (Supporting Information) indicates the thickness of the CIPS nanoflake is 161.8 nm (Figure S4b, Supporting Information), similar to those used in devices (130–170 nm). Figure S4c,d (Supporting Information) shows the PFM amplitude and phase maps of the indicated region. Moreover, the well-defined butterfly loop of the PFM amplitude–voltage curve in Figure S4e (Supporting Information) and the distinct 180° switching of the phase-voltage curve in Figure S4f (Supporting Information) corroborate the robust ferroelectric polarization in the CIPS nanoflake.[42] In addition, the small coercive voltage (±4 V) observed in the hysteresis loop suggests that the polarization orientation in CIPS nanoflakes can be effectively modulated by a relatively small gate voltage. For comparison, we also prepared a standard Te FET, which is shown in Figure S5a (Supporting Information), a bottom metal gate/CIPS/Te heterostructure (Figure S5d, Supporting Information) in metal-ferroelectric-semiconductor (MFS) architecture, and a bottom metal gate/CIPS/h-BN/Te heterostructure (Figure S5g, Supporting Information)) in metal–ferroelectric–insulator–semiconductor (MFIS) architecture, respectively. The fabrication processes were similar to that for the MFMIS device.

2.2. Electrical Pulse Triggered Long-Term Memory Behavior of the MFMIS Device

The electrical measurements of the MFMIS device and other control-group devices were conducted in vacuum at room temperature. At first, we kept the internal gate floating and the bottom gate was electrically biased to trigger the long-term memory behavior of the MFMIS device. **Figure 2** shows the electrical performance of the MFMIS device in Figure 1b, and the source/drain bias (V_{ds}) was kept as 100 mV. Although limited by the narrow band gap of the chosen Te channel, the on/off ratio of the fabricated memory device is not comparable to a conventional FET, which often requires an $I_{on}/I_{off} > 10^3$ for logic circuit operation,[3] our device aiming at in-sensor RC systems presents a similar operation with ferroelectric FET (FeFET).[51] In Figure 2a, the transfer characteristic shows a clockwise hysteresis loop, opposite to the anti-clockwise direction in previous reported *p*-type floating-gate FET[52] and the basic Te FET as shown in Figure S4b (Supporting Information), that illustrates the memory behavior of the MFMIS device roots on the ferroelectric dielectric rather than the trapping states from the floating gate or channel/dielectric interface. To further prove the trivial effect of charge trapping states at the interface between h-BN layer and Te nanoflake in our MFMIS device, the transfer characteristics of the internal Gr/h-BN/Te FET was measured by floating the bottom gate and sweeping the internal gate voltage (V_{int}). Figure S6a,b (Supporting Information) shows the optical microscope image and the schematic illustration of the embedded Gr/h-BN/Te FET, respectively. Figure S6c (Supporting Information) shows the anti-clockwise hysteresis loop with a near-zero memory window, indicating the trivial charge trapping effect at the interface, that is a result of the clean interface between h-BN and Te nanoflakes proved by previous cross-section TEM results. The linear output characteristics in Figure 2b (for the MFMIS device) and Figure S6d (for the internal Gr/h-BN/Te FET; Supporting Information) imply the realization of the ohmic contact between the source/drain electrodes and the channel material. Figure 2c–f illustrates the evolution of the channel conductance variation of the MFMIS device driven by electrical pulses. The impact of pulse width (t_{pulse}) on the conductance evolution is shown in Figure 2c. Different electrical pulses with the amplitude of −5 V and t_{pulse} ranging from 1 ms to 10 ms were applied to the bottom gate. At the t_{pulse} of 1 ms, the excited current reaches a value of 0.175 μA μm^{-1} and shows no degradation in 50 s. When t_{pulse} further increases to 2 ms, the post-stimulus current further reached a value of 0.343 μA μm^{-1}. However, when t_{pulse} is longer than 5 ms, there is no significant difference in the excited current triggered by electrical pulses. This can be explained by the saturation of the downward polarization in the CIPS layer induced by the negative electrical pulse with a long pulse width. Figure 2d–f demonstrates that the conductance states variation of the MFMIS device can be flexibly tuned by using different programming conditions. Besides the pulse width, the pulse amplitude could also effectively modulate the channel conductance. Figure 2d shows the evolution of the conductance variation of Te channel triggered by different electrical pulse sequences with the amplitude of −3, −4, −5, and −6 V, respectively. Each sequence includes ten pulses, the pulse width and interval are 1 ms and 1 s, respectively. It's obvious that a larger pulse amplitude would lead to a higher current. In addition, the channel conductance variation could be enhanced by increasing the pulse number, as shown in Figure 2e. The pulse amplitude, width, and interval are −5 V, 1 ms, and 1 s, respectively. With the increase of the pulse number, the channel conductance experiences a stair-stepping increase, which is

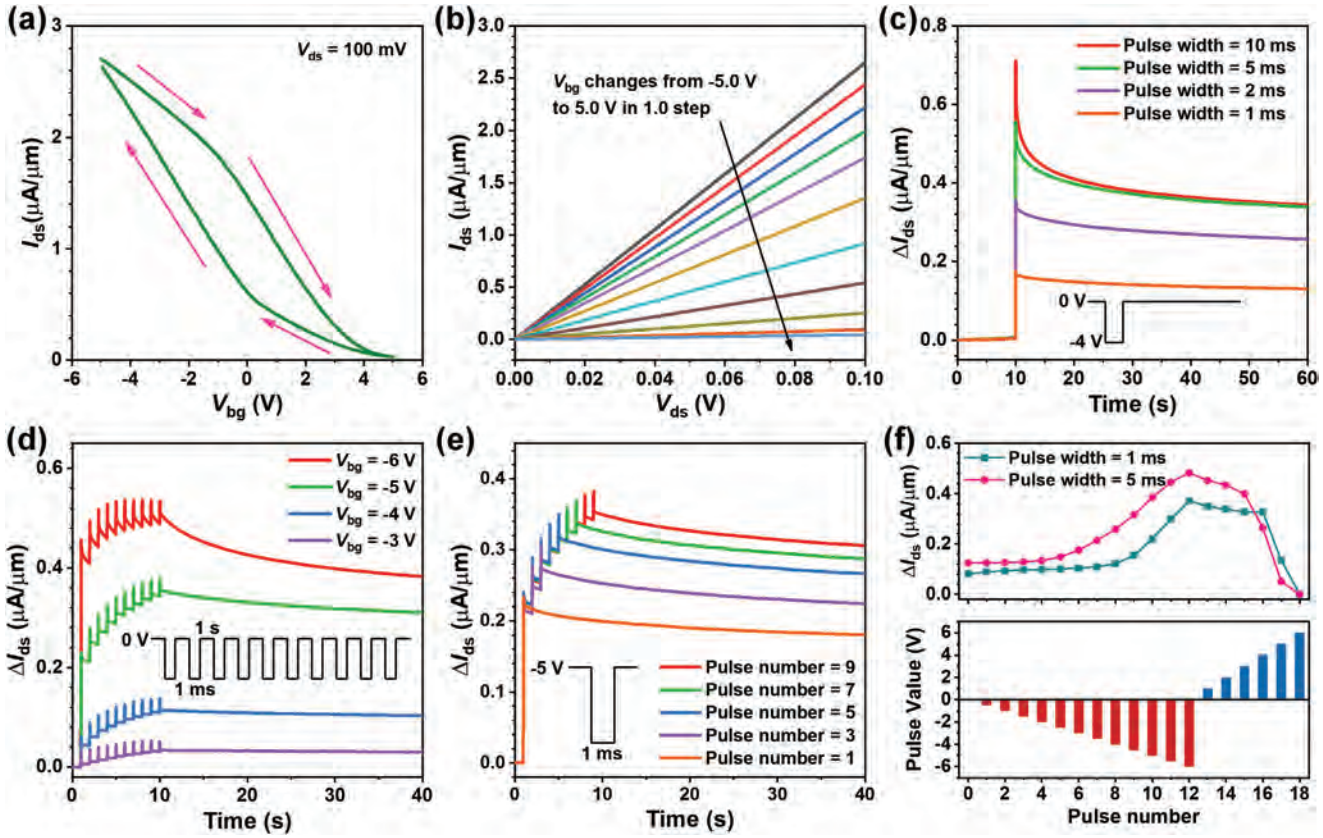

Figure 2. Electrical pulse triggered memory behavior of the MFMIS device. a) Transfer curve of the MFMIS device under the bias of 100 mV. b) Output curves of the MFMIS device. The back-gate voltage V_{bg} increases from −5 V to 5 V with a step of 1 V. c–e) Evolution of the channel conductance variation of the MFMIS device triggered by electrical pulses with c) different pulse width (amplitude: −4 V), d) different amplitude (pulse width: 1 ms, pulse interval: 1 s), and e) different pulse number (amplitude: −5 V, pulse width: 1 ms, pulse interval: 1 s). The readout bias was kept as 100 mV and the internal gate was floating. f) Evolution of the channel conductance variation of the memory device (the top panel) triggered by programmed electrical pulse sequence (the bottom panel) with different pulse widths (1 ms (dark cyan) and 5 ms (pink)).

vtial to the fast learning of the readout map of the RC as to be discussed. On the contrary, the channel conductance could also be depressed by applying the positive electrical pulses, as shown in Figure 2f. The reason behind this is that the polarization in the ferroelectric CIPS nanoflake could be flexibly tuned by changing the pulse amplitude, width, number, and polarity. Specifically, when the absolute pulse amplitude is larger than the coercive voltage, the negative (positive) electrical pulse would potentiate (depress) the channel conductance, and the potentiation (depression) rate would be positively related to the pulse amplitude, width, and number.

The physical mechanism responsible for the memory behavior in the MFMIS device triggered by electrical pulses is schematically illustrated in **Figure 3**a–f. During the application of a negative electrical pulse to the bottom gate, the polarization in the CIPS layer would be driven to point downward under the external electric field. The graphene layer stacked on top of the CIPS layer would help to effectively eliminate the residual depolarization field induced by the compensating charge at the interface of the ferroelectric layer,[43,44] thus enhancing the polarization field in the CIPS layer (Figure 3a). After applying the negative electrical pulses, the downward polarization in CIPS would be retained to keep the accumulation of holes in the Te channel (Figure 3b), corresponding to the long-term low-resistance state. The schematic band diagram in Figure 3c depicts the band bending of the semiconducting Te channel induced by the polarization field in CIPS after applying the negative electrical pulses. On the other hand, the positive electrical pulse would drive the upward polarization in CIPS and lead to the depletion of holes in the Te channel (Figure 3d), corresponding to the high-resistance state. Similarly, the graphene layer also contributes to the elimination of the residual depolarization field. After applying the positive electrical pulses, the upward polarization field would keep the Te channel in the high-resistance state for a long period.

Besides, the effects of the CIPS and graphene layer on the memory behavior in the MFMIS device were studied in the control groups (Figures S5–S7, Supporting Information). For the effect of the ferroelectric CIPS layer, electrical pulses were applied to the graphene gate to trigger the internal Gr/h-BN/Te FET (Figure S6e, Supporting Information), the pulse amplitude, width, and interval of the input pulses were −5 V, 1 ms, and 1 s, respectively. Compared with the MFMIS device, no distinct multistate conductance evolution was observed in the internal Gr/h-BN/Te FET (Figure S6f, Supporting Information), illustrating

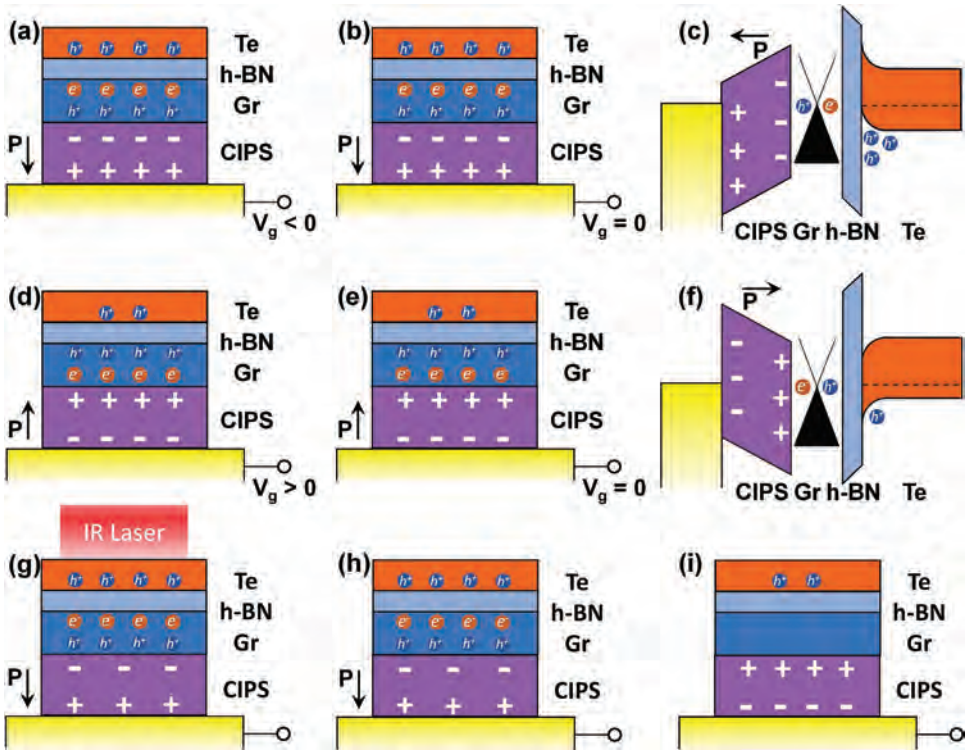

Figure 3. Schematic demonstration of the electronic memory behaviors of the MFMIS device. a–c) Low resistance of Te channel induced by a negative electrical pulse ($V_g < 0$ V). a) The negative electrical pulse input on the bottom gate leads to the downward polarization in the CIPS layer. b) When the electrical pulse is removed, the downward polarization in the CIPS layer could be maintained to keep the low resistance of Te channel. c) The band diagram and the charge distribution in different layers after the excitation of the negative electrical pulse. d–f) High resistance of Te channel induced by a positive electrical pulse ($V_g > 0$ V). d) The positive electrical pulse induces the upward polarization in CIPS layer. e) The high resistance of Te channel is kept by the upward polarization in CIPS layer after removing the positive electrical pulse. f) The band diagram and the charge distribution in different layers after the excitation of the positive electrical pulse. g–i) Resistance evolution of Te channel induced by IR laser. g) Under the excitation of the laser pulse, the photogenerated holes are accumulated in Te channel, inducing the metastable downward polarization in CIPS layer. h) The induced metastable downward polarization can maintain the low-resistance state of Te channel after removing the IR laser. i) The resistance of Te channel gradually returns to its initial value due to the relaxation of the metastable polarization.

the indispensable role of CIPS in the memory behavior of the MFMIS device. To uncover the critical role of graphene in the enhancement of polarization field in CIPS, the electrical performance of Metal/CIPS/Te (MFS) and Metal/CIPS/h-BN/Te (MFIS) devices was studied (Figure S5d–i, Supporting Information). Similar to the MFMIS device, the transfer characteristics of MFS and MFIS devices exhibit the clockwise hysteresis loops (Figure S5e,h, Supporting Information), rather than the anti-clockwise loop in that of the basic Te FET (Figure S5b, Supporting Information). Such difference could be attributed to the polarization switching in the ferroelectric layer triggered by the external electric field. The linear output curves under various bottom gate voltages in Figure S5c,f,i (Supporting Information) show good contacts realized in these devices. Different from the long-term conductance retention behavior in the MFMIS device, the currents in MFS and MFIS devices would not be maintained and relaxed to the initial value within 1 min (Figure S7, Supporting Information). The short retention time could come from the residual depolarization field due to the absence of the graphene layer in these devices.

To demonstrate the application potential of the MFMIS device as the memory unit in the readout layer in the RC system, we study its long-term retention stability and temperature-dependence performance. The long-time retention stability is shown in Figure S8 (Supporting Information), where the low-resistance state was programmed by a −8 V/1 ms electrical pulse, and the high-resistance state was programmed by a +8 V/1 ms electrical pulse, the readout bias was kept as 100 mV. Out of the purpose of pursuing IR photosensitivity, we selected the emerging vdW material Te with a narrow bandgap (≈0.35 eV) as the channel, resulting in a moderate on/off ratio, but the distinct memory states written by electrical pulse can be maintained for more than 11 000 s. At 10 000 s, the current decay is less than 0.02 μA μm^{-1} (≈0.5%) and the noise is negligible. On the other hand, the thermal stability of the MFMIS device demonstrates that our device can work in a relatively harsh environment (Figure S9, Supporting Information). Our measurement system is photographed in Figure S9a (Supporting Information). As shown in Figure S9b (Supporting Information), the transfer curves measured at different temperatures even up to 60 °C show no obvious degradation and after the thermal shock, the device still exhibits long-term retention stability (Figure S9c, Supporting Information). These results demonstrate that the MFMIS device itself can serve as the memory unit in the readout layer of an RC system.

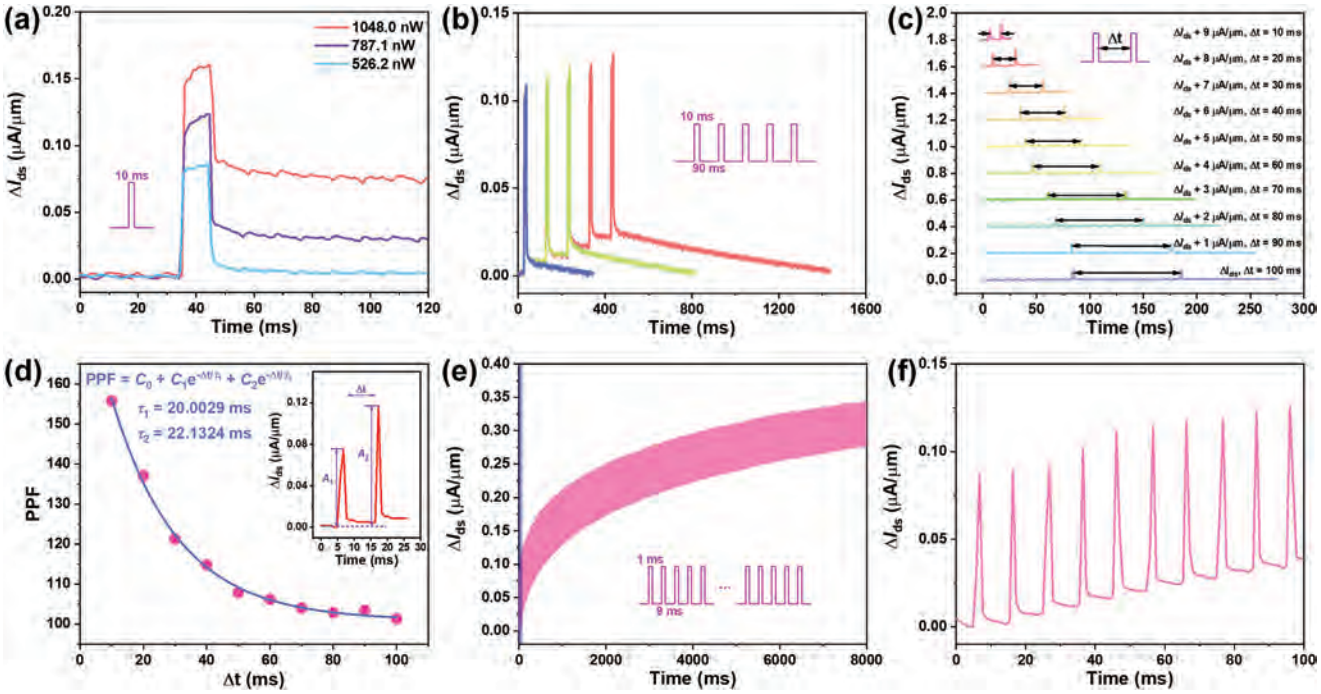

Figure 4. 1550-nm laser pulse triggered memory behavior of the MFMIS device. a) 1550-nm laser pulse triggered channel conductance variation with different laser power (pulse width: 10 ms). b) 1550-nm laser pulse triggered channel conductance variation with different pulse number (pulse width: 10 ms, pulse interval: 90 ms, laser power: 623.1 nW). c) Channel conductance variation triggered by paired optical pulses with different interval (pulse width: 10 ms, laser power: 623.1 nW). d) PPF ratio defined as $(A_2 - A_1)/A_1 \times 100\%$ as a function of the pulse interval, where the blue line is the fitting curve using the double exponential decay function. Inset: PPF effect induced by paired optical pulse. e) Multiple conductance state variation triggered by 1550-nm pulse train. The laser power, pulse width, and pulse interval were 623.1 nW, 1 ms, and 9 ms, respectively. f) Zoom-in conductance variation evolution triggered by the first 10 laser pulses indicated by transparent royal in (e). The readout bias was kept as V_{ds} = 100mVand both internal gate and bottom gate were floating.

2.3. Optical Pulse Triggered Short-Term Memory Behavior of the MFMIS Device

As an emerging vdW semiconducting material, Te has been widely utilized in optoelectronic devices with superior photoresponse in the SWIR region covering the optical communication band (1260–1675 nm).[37–41] The reported photoresponsivity and specific detectivity of the photoconductor based on Te nanoflakes could reach 13 A W^{-1} (1.4 µm) and 2×10^9 Jones (1.7 µm), respectively.[37,40] In consideration of the 1550 nm laser is not only mostly used in optoelectronic laboratories and locates at the C-band for optical fiber communication, we chose the 1550 nm laser pulses as the driving source in our measurements. The integrated Te channel and ferroelectric dielectric in our MFMIS device enables it to practice optical pulse-triggered short-term memory at 1550 nm. **Figure 4** shows the evolution of the conductance variation of the MFMIS device triggered by 1550-nm laser pulses at ambient conditions. During the measurement, V_{ds} was 100 mV, and the internal gates were floating. The diameter of the used laser spot was around 2 mm. Before each measurement, a positive electrical pulse (+5 V) was applied on the bottom gate to help switch the polarization in CIPS to be upward, and then we removed the probe on the bottom gate and kept the bottom gate floating to avoid the additional potential from the external circuit to affect the polarization reversal. The dependence of laser pulse-triggered photocurrent variation on laser power is shown in Figure 4a. By increasing the laser power from 526.2 nW to 1048.0 nW, the peak value of photocurrent increases accordingly, followed by the gradual current decay at different rates. Besides, we also demonstrate that the photocurrent evolution is related to the laser pulse number, which is shown in Figure 4b, where the laser power is 623.1 nW, pulse width and interval are 10 and 90 ms, respectively. With increasing pulse number, the photocurrent can be accumulated and the decay time increases as well. Figure 4c depicts the paired-pulse facilitation (PPF) effect triggered by laser pulse and the PPF ratio as a function of the pulse interval is illustrated in Figure 4d. The pulse width and laser power are 10 ms and 623.1 nW, respectively. The PPF ratio is defined as $(A_2 - A_1)/A_1 \times 100\%$ as shown by the inset in Figure 4d and the blue line represents the fitting results using double exponential decay function: $\mathrm{PPF} = C_0 + C_1 e^{-\Delta t/\tau_1} + C_2 e^{-\Delta t/\tau_2}$, where the time constant τ_1 = 20.0029ms and τ_2 = 22.1324ms. Figure 4e shows the photocurrent evolution triggered by laser pulse train with the frequency of 100 Hz, the duty ratio is 10% (pulse width and pulse interval are 1 ms and 9 ms, respectively). In this characterization, the laser power was kept as 623.1 nW. To provide more details, we zoom in photocurrent evolution triggered by the first ten laser pulses in Figure 4f. To clarify the role of the MFMIS device in the short-term memory behavior triggered by laser pulses, the photoresponse was also measured in the basic Te FET under 1550-nm laser pulses (Figure S10, Supporting

Information, the inset is the optical microscope image of the measured device). For the basic Te FET, the channel current would return to the initial value immediately after the pulse excitation, which is consistent with the previous report[37] and different from the gradual decay behavior in the MFMIS device.

Different from the long-term current potentiation/depression triggered by electrical pulses, the photocurrent triggered by optical pulses decays to its initial value in a short time. The working mechanism behind this phenomenon is similar to the optically induced short-term plasticity based on $PbZr_{0.2}Ti_{0.8}O_3$ (PZT: a ferroelectric thin film)/WS_2 heterostructure using relatively low-intensity light excitations reported by Luo et. al.[27] This optically induced short-term memory behavior in the MFMIS device is attributed to the interplay between the photo-induced charges in the semiconducting channel and polarization charges in the ferroelectric dielectric. It is reasonable for us to postulate that most of the incident IR light was absorbed by the Te channel, and the transmitted part would not induce the polarization reversal in CIPS, that is the direct impact of the laser pulse on the CIPS is negligible. It's worth pointing out that the bandgap of CIPS is large (≈2.62 eV) and it cannot absorb IR light directly.[48] Before shining the laser, the polarization in CIPS dielectric has been switched to be upward by a positive electrical pulse in advance, and thus the Te channel is in high-resistance state. Under the exposure to the 1550-nm laser pulses, electron-hole pairs are generated in the Te channel. Due to the *p*-type nature of the Te channel, holes possess a longer lifetime than electrons, resulting in a net hole accumulation at the h-BN/Te interface (Figure 3g). The accumulated holes would induce a built-in field in the graphene layer, causing the polarization reversal in the CIPS layer, as shown in Figure 3g. After removing the laser pulses, this downward polarization in the CIPS layer would keep the Te channel at the low-resistance state (Figure 3h). However, because of the existence of h-BN and graphene nanoflakes between the semiconducting channel and ferroelectric dielectric, the interplay between the photoinduced charges in Te and polarization charges in CIPS is weak, that is the induced polarization is in metastable state. As shown in Figure 3i, after the laser excitation, photogenerated carriers quickly recombine, which would return the CIPS layer and the Te channel to the initial polarization state and high-resistance state, respectively.

This explanation can be indirectly proved by the comparison between the photocurrent evolution in MFMIS device using electrical pulse to set the polarization in CIPS in different directions in advance. The results are shown in Figure S11 (Supporting Information). When the polarization in CIPS was set to be downward by applying a negative electrical pulse on the bottom gate in advance, there is no obvious optical memory effect even with stronger laser power. In stark contrast to that, with the polarization in CIPS setting to be upward in advance, the desired optical memory behavior is obtained.

2.4. In-Sensor Reservoir Computing at the Optical Communication Band

Combining the long-term memory behavior triggered by electrical pulses and short-term memory behavior triggered by 1550-nm laser pulses, we propose a fully memristive in-sensor reservoir computer that can directly learn and infer from optical fiber signals, rather than using dedicated optical transducers and digital computers. First of all, we can use MFMIS as the memory unit in the readout layer of the RC system. Figure S12 (Supporting Information) presents multi-bit potentiation and depression states triggered by two pulse trains in the MFMIS device. Triggered by 100 negative electrical pulses with an amplitude of −5 V and pulse width of 10 µs, multi-level potentiation states were observed, corresponding to more than 6-bit potentiation states. On the other hand, close to 8-bit depression states were also recorded during applying 200 positive electrical pulses with an amplitude of 4 V. This pulse number controlled multi-bit states lay the foundation for the real-time learning capability of the in-sensor RC system based on the MFMIS device. Next, utilizing the optically induced short-term memory behavior, the 4-bit vector encoding was demonstrated in the MFMIS device (Figure S13, Supporting Information). In this characterization extraction, the used laser power was 616.4 nW and the pulse frequency was 0.5 Hz, duty ratio was 10% (t_{pulse} = 200 ms). As indicated by the inset, "0" and "1" correspond to the on and off states of the laser pulse, respectively. By programming the device with all possible pulse trains ("0001" to "1111"), 15 different volatile memory states were recorded at the end of each pulse train. The initial current without the exposure to laser pulse was identified as the memory state programmed by "0000" pulse train. The ability to encode different optical signals into multi-level memory states in the MFMIS device under 1550-nm laser pulse stream is an integral of in-sensor RC system at the optical communication band.

The schematic illustration of this in-sensor reservoir computer is shown in the left panel of **Figure 5**a, which consists of the input layer, middle layer, and output layer. The input layer receives data in the form of optical pulses transmitted by optical fiber at a wavelength of 1550 nm before being sensed by our MFMIS devices. The middle layer, also known as the "reservoir", is composed of multiple nodes or memory devices that map complex input signals to reservoir states for feature extraction. The linear output layer makes use of the extracted features to accomplish tasks such as classification and regression. In RC, the input and the middle layer remain fixed, only the weights of the readout layer need to be trained. Therefore, it features very low training cost that substantially benefits learning at the edge.

The right panel of Figure 5a shows the schematic illustration of the MFMIS device-based in-sensor reservoir for classifying temporal sequences, using the representative MNIST handwritten digits dataset as an example. The optical stimuli representing MNIST handwritten digits are transmitted through the optical fiber, which directly excites the memory devices without associated analogue-to-digital data conversion. The absence of extra optical sensors and data conversion benefits the energy and time consumption considerably, representing a major advantage of the optoelectronic in-sensor RC method over traditional RC. This improvement is attributed to our MFMIS that physically encodes the optical fiber signal into its conductance thanks to the optical signal-triggered short-term memory behavior. In our simulated setup, each MNIST handwritten digit image has 28×28 pixels. A preprocessing

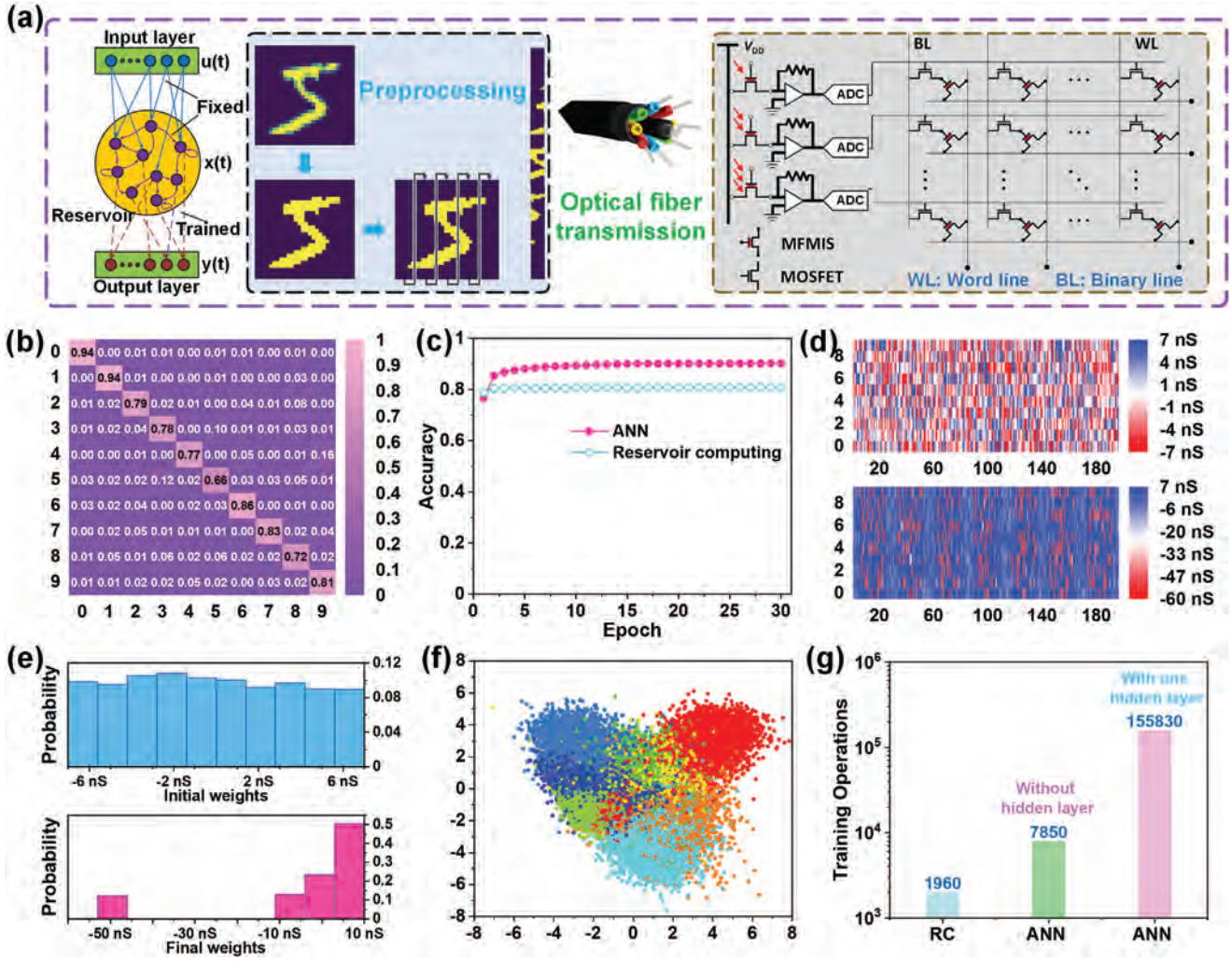

Figure 5. In-sensor RC system at the optical communication band based on the MFMIS device. a) Schematic illustration of the RC system for classifying the MNIST dataset (MFMIS: MFMIS device; MOSFET: metal-oxide-semiconductor field-effect transistor). b) Confusion matrix on classifying the MNIST test set. c) In-situ learning performance of the RC network over epochs, using 60 000 handwritten digits for training and 10 000 digits for testing. The pink and cyan dots correspond to the classification accuracy of software and MFMIS device-based RC system, respectively. d) Initial (top panel)/final (bottom panel) device crossbar array conductance before/after training. e) Initial (top panel)/final (bottom panel) corresponding device crossbar array conductance distributions of d) before/after training. f) Dimensionality reduction of optoelectronic reservoir outputs using linear discriminative analysis (LDA). g) Number of training operations for RC, artificial neural network (ANN) without hidden layer and with one hidden layer, respectively, showing RC significantly reduces the training complexity.

was performed before the images were transmitted through optical fiber bundle into the reservoir. Take the image of digit 5 as an example, the original image was first trimmed, followed by binarization into a black and white image. The columns were then divided into five groups where each group consists of four adjacent columns. The column groups were then concatenated to form a 110×4 matrix. Each row of the matrix, or a 4-bit row vector, corresponds to one of the 16 illumination patterns in Figure S9 (Supporting Information). In this case, the conductance of each memory device right after receiving optical fiber stimulation will thus encode a small patch of the original image. The collective device states, representing the reservoir state, can be used to perform pattern recognition through the trained readout function, in our case to identify corresponding digit of the image that was transmitted by the optical fiber.

The corresponding currents for each row were then fed to the readout map for classification. A fully connected layer served as the role of the readout, which was simulated using a crossbar array of electrically operated MFMIS devices for the digit classification. The gradients computation for the readout layer was in software and the MFMIS device conductance update was simulated according to the long-term memory behavior governed by pulse number. The conductivity was updated by minimizing a cross-entropy loss function. Figure 5b shows the confusion matrix in classifying the MNIST test set, which is dominated by the diagonal elements, indicating the robustness of the system although digit 5 exhibits weak confusion with digit 9. The training results are summarized in Figure 5c. The pink dots in the figure represent the epoch-wise classification accuracy in software, and the cyan dots are the results of the in-sensor

RC with the MFMIS devices, comparable to the software baseline. The initial and final conductance of the electrically operated memory devices in the readout layer and their distributions are shown in Figure 5d,e, respectively. Please refer to the supplementary information for details about how to map the conductance to the weights of the readout map. Figure 5f illustrates the 2D distribution of the extracted feature vectors produced by the optoelectronic reservoir using linear discriminant analysis (LDA) for dimensionality reduction. It is observed that the encoded features have well clustered in the 2D space thanks to the nonlinear transformations by the short-term memory of optically operated memory devices.

A significant advantage of using RC system is the reduction of training cost. As shown in Figure 5g, for this task, a conventional two-layer fully connected neural network of 110 hidden units (same with the number of reservoir nodes) will possess 155 830 weights to be trained. This number will grow very quickly if the network goes deeper but retains a constant for the RC, affirming the advantage of RC for affordable real-time edge learning.

In addition, we also studied the effect of the current variation noise collected from the MFMIS device on the identification accuracy in the RC system and the result is that with considering noise, the accuracy is 0.011 lower than that without considering noise. More detailed discussion please refer to Figure S14 (Supporting Information).

3. Conclusions

In summary, we have reported an electronic/optoelectronic dual-responsive memory device in an MFMIS architecture (metal/CIPS/Gr/h-BN/Te), where the semiconducting Te nanoflake serves as the IR photoactive channel and the ferroelectric CIPS nanoflake is the functional layer to introduce the memory behavior by modulating the conductance of the Te channel. In addition, the graphene layer can compensate the ferroelectric polarization in the CIPS layer, and the h-BN nanoflake serves as the insulating dielectric layer. The fabricated MFMIS device manifests both long-term and short-term memory behaviors driven by electrical pulses and optical pulses in SWIR region, respectively. Moreover, the underlying mechanism of the observed memory behaviors in the MFMIS device was systematically studied by comparing the memory behaviors in devices with the metal/CIPS/Te (MFS) and the metal/CIPS/h-BN/Te (MFIS) architectures. Based on the MFMIS device, we proposed a fully memristive in-sensor RC system at the optical communication band with 1550-nm laser as the representative light source, featuring co-location of sensing, processing, and memory. Such a system combines the role of transducer, message decoder as well as AI accelerator, evidenced by its capability to directly learn and classify MNIST images transmitted through the optical fiber. Specifically, under the electrical pulses, the MFMIS devices can exhibit the long-term memory behavior with the multi-bit potentiation and depression states, serving as the readout layer of the proposed in-sensor RC system. Owing to the short-term memory behavior triggered by the optical pulses, the MFMIS devices encode the optical signals, functioning as the reservoir nodes to extract features of bit streams. This MFMIS device-based in-sensor RC system paves the way for energy-efficient, compact, and smart signal processing systems for real-time edge computing.

4. Experimental Section

Heterostructure Preparation and Device Fabrication: h-BN and graphite single crystals were purchased from the 2D Semiconductor Inc. High-quality CIPS single crystals were synthesized via a chemical vapor transport method, which is similar to previous reports.[42,53] Te nanoflakes were synthesized via a hydrothermal method.[32,37] In the preparation of the heterostructures, all the vdW nanoflakes except for Te nanoflakes were first mechanically exfoliated onto the Si/SiO_2 substrate (SiO_2: 300 nm). For Te nanoflakes, the final product of the hydrothermal synthesis was drop-casted onto the Si/SiO_2 substrate. The bottom Cr/Au (5/100 nm) gate was deposited onto the Si/SiO_2 (SiO_2: 300 nm) substrate by a thermal evaporation method. When all the ingredients were ready, the heterostructures in different architectures were prepared by stacking these vdW nanomaterials layer by layer on a Cr/Au bottom gate via a wet transfer method.[46] Finally, the source/drain and internal gate electrodes were defined by the standard electron beam lithography process (TESCAN, VEGA3) followed by the thermal evaporation of 100-nm Au. The CIPS nanoflakes used to conduct the out-of-plane PFM measurement were exfoliated onto a Si/SiO_2 substrate covered with a Cr (5 nm)/Au (50 nm) metal layer.

Device Characterizations: The optical microscope images of these devices were captured by an optical microscope (Nikon, EBLIPSE LV100ND). The height profiles of the vdW nanoflakes in these heterostructures were characterized by the atomic force microscope (AFM) (Bruker, Dimension Icon with Scan Asyst). The Raman spectra were obtained by a Renishaw Raman Microscope with the excitation of 532-nm polarized laser at room temperature. The PFM measurements of the CIPS nanoflakes were carried out on the Asylum Cypher ES in the scanning mode of SSPFM. The electrical pulse-triggered conductance evolutions of these devices were characterized on a cryogenic probe station (LakeShore) in vacuum with a source meter (Keysight B2902B). The characterization of the long-term retention performance was conducted on the same probe station in vacuum. The channel current was monitored by a B1500A semiconductor analyzer around 1 min after the electrical pulses which were generated by a source meter (Keysight B2902B). The optical pulse-triggered conductance evolution of the MFMIS devices was conducted by a home-made optoelectronic characterization platform under ambient conditions, where the 1550-nm optical pulses were provided by a monochrome laser and guided to the device via an optical fiber, and the triggered current was monitored by an Agilent 4155 C semiconductor analyzer (Agilent Technologies, Santa Clara, CA).

Simulation of the In-Sensor Reservoir Computing System with the MFMIS Devices: The simulated in-sensor RC system consists of 110 optically operated memory devices serving as the reservoir nodes, followed by a 110×4 electrically operated memory devices crossbar array that implements a fully connected layer. This conductance programming by both optical and electrical stimulus is calibrated using experimentally acquired single-device measurement data. The learning is carried out by minimizing the categorical cross-entropy loss using a mini-batch (batch size = 128) gradient descent with the Adam optimizer (initial learning rate = 0.01, step size = 15, gamma = 0.1). To electrically program MFMIS device crossbar array, the estimated gradient was first converted to the number of pulses (multiplying a factor and rounding), the corresponding resultant conductance was estimated according to Figure S6 (Supporting Information). The updated conductance was used in the subsequent forward pass for the in-situ training of the readout layer. All 60000 handwritten digits in the training set were used in the learning epochs and the 10 000 digits of the test set were used for inference.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

C. Tan, H. Zhang and J. Zha have filed a patent application related to the memory device reported in this work.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D tellurium, in-sensor reservoir computing, optical communication band, optoelectronic memory device, van der Waals heterostructures

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[1] C. Tan, X. Cao, X.-J. Wu, Q. He, J. Yang, X. Zhang, J. Chen, W. Zhao, S. Han, G. Nam, M. Sindoro, H. Zhang, *Chem. Rev.* **2017**, *117*, 6225.
[2] C. Chang, W. Chen, Y. Chen, Y. Chen, Y. Chen, F. Ding, C. Fan, H. J. Fan, Z. Fan, C. Gong, Y. Gong, Q. He, X. Hong, S. Hu, W. Hu, W. Huang, Y. Huang, W. Ji, D. Li, L.-J. Li, Q. Li, L. Lin, C. Ling, M. Liu, N. Liu, Z. Liu, K. P. Loh, J. Ma, F. Miao, H. Peng, et al., *Acta Phys. Chim. Sin.* **2021**, *37*, 2109017.
[3] Z. Lin, Y. Huang, X. Duan, *Nat. Electron.* **2019**, *2*, 378.
[4] K. Zhu, C. Wen, A. Aljarb, F. Xue, X. Xu, V. Tung, X. Zhang, H. Alshareef, M. Lanza, *Nat. Electron.* **2021**, *4*, 775.
[5] X. Xu, Y. Ding, S. X. Hu, M. Niemier, J. Cong, Y. Hu, Y. Shi, *Nat. Electron.* **2018**, *1*, 216.
[6] G. Migliato Marega, Y. Zhao, A. Avsar, Z. Wang, M. Tripathi, A. Radenovic, A. Kis, *Nature* **2020**, *587*, 72.
[7] F. Zhou, Y. Chai, *Nat. Electron.* **2020**, *3*, 664.
[8] R. Chau, B. Doyle, S. Datta, J. Kavalieros, K. Zhang, *Nat. Mater.* **2007**, *6*, 810.
[9] Z. Wei, *Nat. Electron.* **2022**, *5*, 715.
[10] W. Maass, T. Natschläger, H. Markram, *Neural Comput* **2002**, *14*, 2531.
[11] C. Du, F. Cai, M. Zidan, W. Ma, S. Lee, W. Lu, *Nat. Commun.* **2017**, *8*, 2204.
[12] J. Moon, W. Ma, J. Shin, F. Cai, C. Du, S. Lee, W. Lu, *Nat. Electron.* **2019**, *2*, 480.
[13] G. Milano, G. Pedretti, K. Montano, S. Ricci, S. Hashemkhani, L. Boarino, D. Ielmini, C. Ricciardi, *Nat. Mater.* **2022**, *21*, 195.
[14] L. Sun, Z. Wang, J. Jiang, Y. Kim, B. Joo, S. Zheng, S. Lee, W. Yu, B. Kong, H. Yang, *Sci. Adv.* **2021**, *7*, eabg1455.
[15] K. Liu, T. Zhang, B. Dang, L. Bao, L. Xu, C. Cheng, Z. Yang, R. Huang, Y. Yang, *Nat. Electron.* **2022**, *5*, 761.
[16] A. Hong, E. Song, H. Yu, M. Allen, J. Kim, J. Fowler, J. Wassei, Y. Park, Y. Wang, J. Zou, R. Kaner, B. Weiller, K. Wang, *ACS Nano* **2011**, *5*, 7812.
[17] M. Sup Choi, G. Lee, Y. Yu, D. Lee, S. Hwan Lee, P. Kim, J. Hone, W. Jong Yoo, *Nat. Commun.* **2013**, *4*, 1624.
[18] P. Cheng, K. Sun, Y. Hu, *Nano Lett.* **2016**, *16*, 572.
[19] Q. Vu, Y. Shin, Y. Kim, V. Nguyen, W. Kang, H. Kim, D. Luong, I. Lee, K. Lee, D. Ko, J. Heo, S. Park, Y. Lee, W. Yu, *Nat. Commun.* **2016**, *7*, 12725.
[20] D. Li, M. Chen, Z. Sun, P. Yu, Z. Liu, P. M. Ajayan, Z. Zhang, *Nat. Nanotechnol.* **2017**, *12*, 901.
[21] Y. Shi, X. Liang, B. Yuan, V. Chen, H. Li, F. Hui, Z. Yu, F. Yuan, E. Pop, H. Wong, M. Lanza, *Nat. Electron.* **2018**, *1*, 458.
[22] M. Wang, S. Cai, C. Pan, C. Wang, X. Lian, Y. Zhuo, K. Xu, T. Cao, X. Pan, B. Wang, S. Liang, J. Yang, P. Wang, F. Miao, *Nat. Electron.* **2018**, *1*, 130.
[23] F. Zhang, H. Zhang, S. Krylyuk, C. Milligan, Y. Zhu, D. Zemlyanov, L. Bendersky, B. Burton, A. Davydov, J. Appenzeller, *Nat. Mater.* **2019**, *18*, 55.
[24] D. Jayachandran, A. Oberoi, A. Sebastian, T. Choudhury, B. Shankar, J. Redwing, S. Das, *Nat. Electron.* **2020**, *3*, 646.
[25] L. Liu, C. Liu, L. Jiang, J. Li, Y. Ding, S. Wang, Y. Jiang, Y. Sun, J. Wang, S. Chen, D. Zhang, P. Zhou, *Nat. Nanotechnol.* **2021**, *16*, 874.
[26] X. Sun, C. Zhu, J. Yi, L. Xiang, C. Ma, H. Liu, B. Zheng, Y. Liu, W. You, W. Zhang, D. Liang, Q. Shuai, X. Zhu, H. Duan, L. Liao, Y. Liu, D. Li, A. Pan, *Nat. Electron.* **2022**, *5*, 752.
[27] Z. Luo, X. Xia, M. Yang, N. Wilson, A. Gruverman, M. Alexe, *ACS Nano* **2020**, *14*, 746.
[28] J. Zha, M. Luo, M. Ye, T. Ahmed, X. Yu, D. Lien, Q. He, D. Lei, J. Ho, J. Bullock, K. Crozier, C. Tan, *Adv. Funct. Mater.* **2022**, *32*, 2111970.
[29] M. Long, P. Wang, H. Fang, W. Hu, *Adv. Funct. Mater.* **2019**, *29*, 1803807.
[30] Z. Shi, R. Cao, K. Khan, A. Tareen, X. Liu, W. Liang, Y. Zhang, C. Ma, Z. Guo, X. Luo, H. Zhang, *Nano-Micro Lett.* **2020**, *12*, 99.
[31] J. Loferski, *Phys. Rev.* **1954**, *93*, 707.
[32] Y. Wang, G. Qiu, R. Wang, S. Huang, Q. Wang, Y. Liu, Y. Du, W. Goddard, M. Kim, X. Xu, P. Ye, W. Wu, *Nat. Electron.* **2018**, *1*, 228.
[33] P. Yang, J. Zha, G. Gao, L. Zheng, H. Huang, Y. Xia, S. Xu, T. Xiong, Z. Zhang, Z. Yang, Y. Chen, D. Ki, J. Liou, W. Liao, C. Tan, *Nano-Micro Lett.* **2022**, *14*, 109.
[34] C. Zhao, C. Tan, D. Lien, X. Song, M. Amani, M. Hettick, H. Nyein, Z. Yuan, L. Li, M. Scott, A. Javey, *Nat. Nanotechnol.* **2020**, *15*, 53.
[35] Y. Yang, M. Xu, S. Jia, B. Wang, L. Xu, X. Wang, H. Liu, Y. Liu, Y. Guo, L. Wang, S. Duan, K. Liu, M. Zhu, J. Pei, W. Duan, D. Liu, H. Li, *Nat. Commun.* **2021**, *12*, 6081.
[36] J. Shen, S. Jia, N. Shi, Q. Ge, T. Gotoh, S. Lv, Q. Liu, R. Dronskowski, S. R. Elliott, Z. Song, M. Zhu, *Science* **2021**, *374*, 1390.

[37] M. Amani, C. Tan, G. Zhang, C. Zhao, J. Bullock, X. Song, H. Kim, V. Shrestha, Y. Gao, K. Crozier, M. Scott, A. Javey, *ACS Nano* **2018**, *12*, 7253.
[38] C. Tan, M. Amani, C. Zhao, M. Hettick, X. Song, D. Lien, H. Li, M. Yeh, V. Shrestha, K. Crozier, M. Scott, A. Javey, *Adv. Mater.* **2020**, *32*, 2001329.
[39] L. Tong, X. Huang, P. Wang, L. Ye, M. Peng, L. An, Q. Sun, Y. Zhang, G. Yang, Z. Li, F. Zhong, F. Wang, Y. Wang, M. Motlag, W. Wu, G. Cheng, W. Hu, *Nat. Commun.* **2020**, *11*, 2308.
[40] M. Peng, R. Xie, Z. Wang, P. Wang, F. Wang, H. Ge, Y. Wang, F. Zhong, P. Wu, J. Ye, Q. Li, L. Zhang, X. Ge, Y. Ye, Y. Lei, W. Jiang, Z. Hu, F. Wu, X. Zhou, J. Miao, J. Wang, H. Yan, C. Shan, J. Dai, C. Chen, X. Chen, W. Lu, W. Hu, *Sci. Adv.* **2021**, *7*, eabf7358.
[41] C. Shen, Y. Liu, J. Wu, C. Xu, D. Cui, Z. Li, Q. Liu, Y. Li, Y. Wang, X. Cao, H. Kumazoe, F. Shimojo, A. Krishnamoorthy, R. Kalia, A. Nakano, P. D. Vashishta, M. Amer, A. Abbas, H. Wang, W. Wu, C. Zhou, *ACS Nano* **2020**, *14*, 303.
[42] F. Liu, L. You, K. Seyler, X. Li, P. Yu, J. Lin, X. Wang, J. Zhou, H. Wang, H. He, S. Pantelides, W. Zhou, P. Sharma, X. Xu, P. Ajayan, J. Wang, Z. Liu, *Nat. Commun.* **2016**, *7*, 12357.
[43] X. Wang, C. Zhu, Y. Deng, R. Duan, J. Chen, Q. Zeng, J. Zhou, Q. Fu, L. You, S. Liu, J. H. Edgar, P. Yu, Z. Liu, *Nat. Commun.* **2021**, *12*, 1109.
[44] M. Chyasnavichyus, M. Susner, A. Ievlev, E. Eliseev, S. Kalinin, N. Balke, A. Morozovska, M. McGuire, P. Maksymovych, *Appl. Phys. Lett.* **2016**, *109*, 172901.
[45] X. Wang, Y. Chen, G. Wu, D. Li, L. Tu, S. Sun, H. Shen, T. Lin, Y. Xiao, M. Tang, W. Hu, L. Liao, P. Zhou, J. Sun, X. Meng, J. Chu, J. Wang, *npj 2D Mater. Appl.* **2017**, *1*, 38.
[46] H. Guo, Z. Hu, Z. Liu, J. Tian, *Adv. Funct. Mater.* **2021**, *31*, 2007810.
[47] Y. Vysochanskii, V. Stephanovich, A. Molnar, V. B. Cajipe, X. Bourdon, *Phys. Rev. B* **1998**, *58*, 9119.
[48] R. Ma, D. Xu, Z. Guan, X. Deng, F. Yue, R. Huang, Y. Chen, N. Zhong, P. Xiang, C. Duan, *Appl. Phys. Lett.* **2020**, *117*, 131102.
[49] A. C. Ferrari, J. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. Novoselov, S. Roth, A. Geim, *Phys. Rev. Lett.* **2006**, *97*, 187401.
[50] R. Geick, C. Perry, G. Rupprecht, *Phys. Rev.* **1966**, *146*, 543.
[51] C. Zhou, Y. Chai, *Adv. Electron. Mater.* **2017**, *3*, 1600400.
[52] D. Li, X. Wang, Q. Zhang, L. Zou, X. Xu, Z. Zhang, *Adv. Funct. Mater.* **2015**, *25*, 7360.
[53] V. Maisonneuve, M. Evain, C. Payen, V. Cajipe, P. Molinié, *J. Alloys Compd.* **1995**, *218*, 157.