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Diameter dependence of electron mobility in InGaAs nanowires

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In this work, we present the diameter dependent electron mobility study of InGaAs nanowires (NWs) grown by gold-catalyzed vapor transport method. These single crystalline nanowires have an In-rich stoichiometry (i.e., $In_{0.7}Ga_{0.3}As$) with dispersed diameters from 15 to 55 nm. The current-voltage behaviors of fabricated nanowire field-effect transistors reveal that the aggressive scaling of nanowire diameter will induce a degradation of electron mobility, while low-temperature measurements further decouple the effects of surface/interface traps and phonon scattering, highlighting the impact of surface roughness scattering on the electron mobility. This work suggests a careful design consideration of nanowire dimension is required for achieving the optimal device performances. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4794414]

Due to high electron mobility and small leakage current, InGaAs nanowires (NWs) have recently attracted tremendous interests as promising n-channel materials for high-performance nanoelectronics.[1–5] For example, vertical wrap-gate transistors with InGaAs NW arrays as the core channel materials have been demonstrated on Si with extraordinary electrical characteristics.[1] In future, the aggressive diameter scaling of NWs will be adopted to further improve the gate electrostatic control as well as lower the off-state current;[6–8] however, this scaling will also inevitably introduce more surface scattering and higher surface carrier recombination, which are detrimental to the transistor behavior.[9,10] In this regard, the dependence of carrier mobility on NW diameters suggests an important design consideration of NW dimension to achieve the optimal device performances. To date, experimental studies on the diameter-dependent electron mobility of Si and InAs NWs[11,12] have illustrated the mobility was reduced significantly for smaller NW diameters while such knowledge in InGaAs NWs is still lacking. In this letter, we present the study of diameter-dependent electron field-effect mobility of In-rich InGaAs NWs, in which the intrinsic electron mobility is found to be monotonically decreased as the NW diameters scale down. The same dependency is also observed at low-temperature current-voltage (I-V) measurement, which further eliminates the influence of acoustic phonon scattering and thermal activated surface/interface traps in this diameter scaling. All these results reveal the impact of surface roughness scattering on the mobility degradation for miniaturized NWs.

The InGaAs NWs used in this study were prepared by a solid-source chemical vapor transport method as previously reported.[3] Briefly, the SiO_2/Si growth substrate (50 nm thermal oxide on degenerately doped Si) was pre-deposited with a 0.5 nm thick Au film as the catalyst and positioned in the downstream of a two-zone furnace. A boron nitride crucible was placed in the upstream containing InAs and GaAs powder mixture in the 1:1 weight ratio. Despite the effective control of chemical stoichiometry in these $In_xGa_{1-x}As$ NWs, we chose the In-rich $In_xGa_{1-x}As$ ($x = 0.7$) NWs in this study due to their intrinsically higher electron mobility.[13] Importantly, the growth process adopted a two-step method to ensure the uniform NW morphology and stoichiometry.[3] As demonstrated in Figures 1(a) and 1(b), the as-grown NWs have smooth surface and length exceeding 10 μm while consisting of a single-crystalline structure with a dominant growth direction of $\langle 111 \rangle$. It should be noted that there is a thin native oxide layer of ~1.5 nm on the NW surface, which will be subtracted from the NW diameters for subsequent mobility determination. The corresponding energy-dispersive X-ray spectroscopy (EDS) spectrum in Figure 1(c) also confirms the In concentration, x, being ~0.7 in our ternary $In_xGa_{1-x}As$ NWs, which is normally obtained in the above-mentioned growth technique.[13]

In order to precisely characterize the diameter of NWs obtained in the same growth run, we performed atomic force microscopy (AFM) study of our NWs, harvested in anhydrous ethanol solution and then drop-casted onto the SiO_2/Si substrates, with three distinctive dimensions. The two-dimensional (2-D) and three-dimensional (3-D) AFM topography images of these representative NWs are shown in Figure 2. It is obvious that all NWs have uniform diameters axially, which are measured as 20.5 (thin), 30.7 (medium), and 40.3 nm (thick), respectively, from the thickness determination (3-D topography). Although the thick NW does not seem thicker than the medium one in the 2-D images, it is typically normal due to the tip radius difference. Also, by tracing along the NW length, the root-mean-square (rms) surface roughness is observed to be 0.5 to 1.0 nm for all

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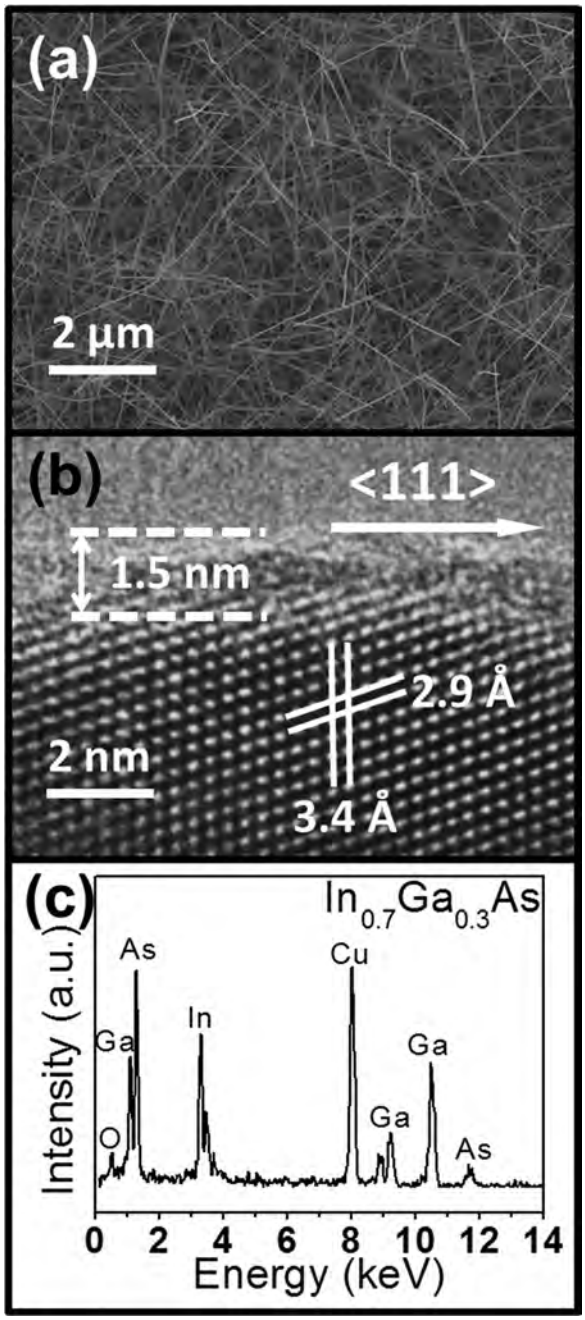

FIG. 1. Electron microscopy characterization of the as-grown NWs. (a) SEM image of the NWs; (b) HRTEM image of a representative NW as depicted in (a); and (c) EDS spectrum of the corresponding NW body, which confirms the chemical stoichiometry being $In_{0.7}Ga_{0.3}As$.

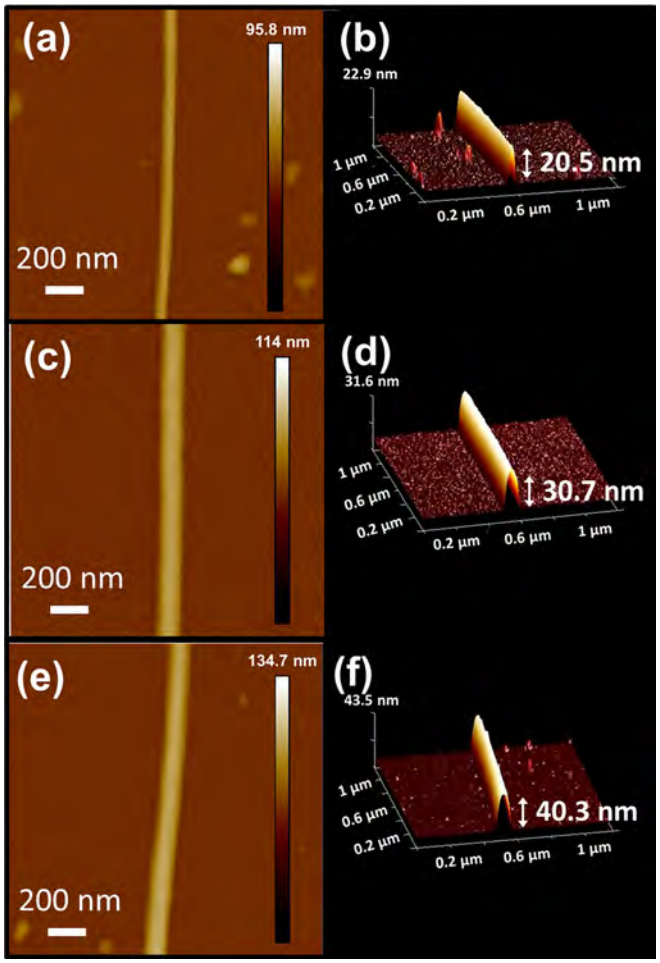

FIG. 2. AFM characterization of different NW channels. (a) 2-D and (b) 3-D AFM topography image of a thin NW channel (d = 20.5 nm and surface roughness = 0.7 nm); (c) 2-D and (d) 3-D AFM topography image of a medium thick NW channel (d = 30.7 nm and surface rougvghness~0.5 nm); and (e) 2-D and (f) 3-D AFM topography image of a thick NW channel (d~40.3 nm and surface roughness~1.0 nm).

NWs characterized, which highly indicates the well-controlled NW surface morphology achieved in our simple growth method as well as the consistent surface roughness of NWs in this comparison study. More importantly, all these findings can lead us to the accurate determination of NW diameters for the mobility calculation.

After characterizing the diameter and morphology, the NW field-effect-transistors (FETs) are then fabricated with standard lithography on drop-casted substrates, followed by the Ni source/drain (S/D) electrode (50 nm thick) deposition and lift-off process. The schematic of such back-gated FET structure is shown in the inset of Figure 3(a), while the main panel contains the transfer characteristics of FETs made of NWs with three different diameters, $d = 19.3$, 32.4, and 41.9 nm, after oxide deduction. Notably, the long channel lengths ($>1\ \mu$m) are used to ensure the diffusive transport of carriers (rather than ballistic or quasi-ballistic transport) assessed in this work, from which intrinsic transport properties, such as carrier mobility, can be deduced. In any case, the normalized current is observed to be higher for the thicker NWs, which could be attributed to the increased effective channel width and more electron transport modes (i.e., subbands) get involved, but the effect of less surface and phonon scattering of larger NWs should not be neglected as well.[12] Furthermore, as depicted in Figures 3(b)–3(d), all devices exhibit the linear I_{DS}-V_{DS} behavior under $V_{DS} = 0.1$ V, which confirms the ohmic contact formation with Ni S/D electrodes for each NW dimension. Combining with the minimized electrical hysteresis observed in this ambient measuring environment (Figure 3(a)), all these can provide a more accurate assessment of the transconductance here.[14–17]

Next, to assess the electron field-effect mobility (μ) of InAs NWs, we utilize the standard square law model, $\mu = g_m(L^2/C_{ox})(1/V_{DS})$, where transconductance $g_m = (dI_{DS})/(dV_{GS})$ at a constant V_{DS} and C_{ox} is the gate capacitance, which is calculated from finite element analysis software

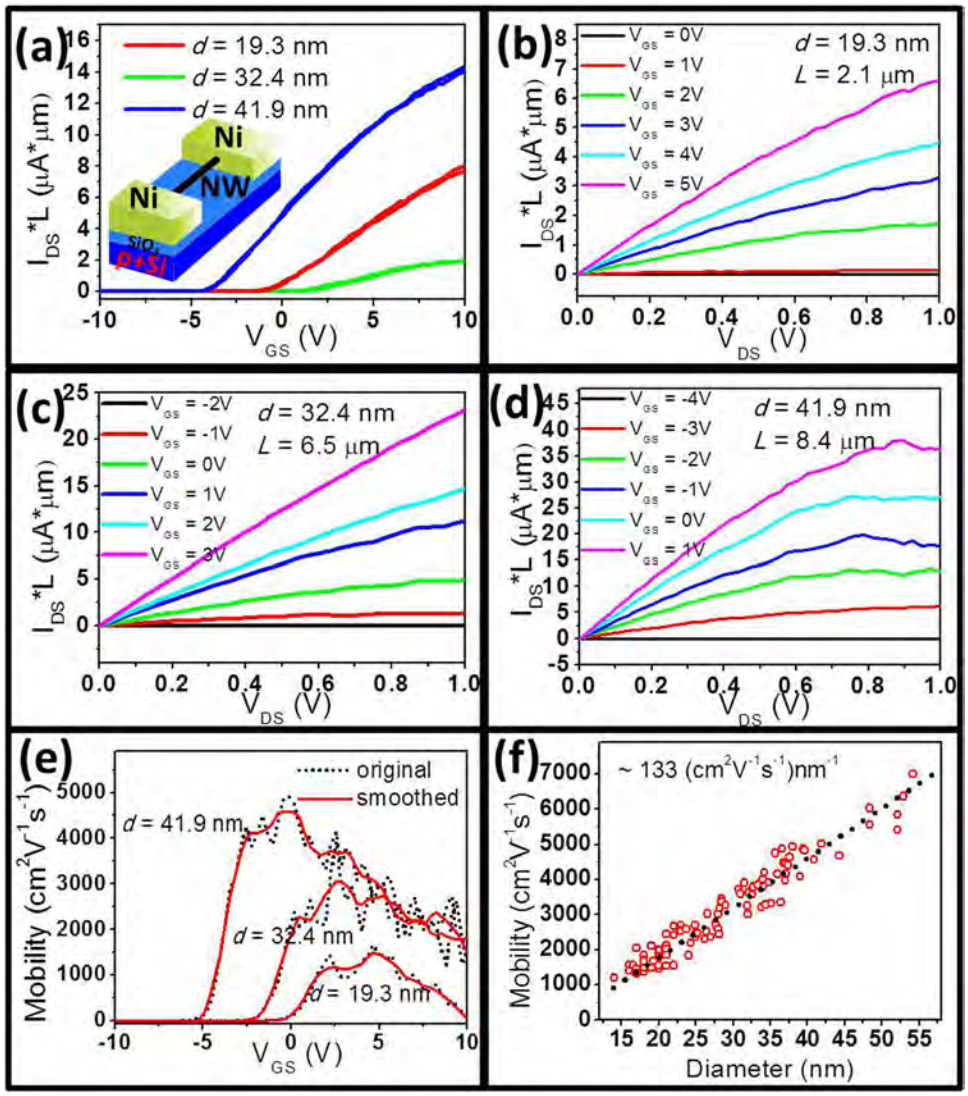

FIG. 3. Electrical characterization of $In_{0.7}Ga_{0.3}As$ NWFETs with different NW dimensions. (a) Transfer characteristic of three back-gated $In_{0.7}Ga_{0.3}As$ NWFETs with different NW diameters (d = 19.3, 32.4, and 41.9 nm, after the native oxide deduction) for $V_{DS} = 0.1$ V. The inset shows the transistor schematic with Ni S/D metal contacts. (b)–(d) Output performance of the three corresponding devices as shown in (a). (e) Field-effect electron mobility assessment for the same set of NWFETs under $V_{DS} = 0.1$ V as presented in (a). The black dotted line is the experiment data while the solid red line is the smoothed data curve. (f) Peak field-effect mobility as a function of NW diameter for ~100 NWs with the diameters ranging from 14 to 54 nm.

COMSOL. As shown in Figure 3(e), the peak mobility is estimated ~4500, 3000, and 1400 $cm^2 V^{-1}s^{-1}$ for these representative thick, medium, and thin NWs, respectively. Besides this clear difference in the mobility, the peak positions of these curves are also distinctive as they are located at ~0, 3, and 5 V for NWs with $d = 41.9$, 32.4, and 19.3 nm, accordingly. This size-dependent phenomenon could be attributed to the higher gate field that leads to an enhanced surface scattering in smaller diameter of NWs.[18,19] More importantly, as demonstrated in Figure 3(f), the statistically summarized peak field-effect mobility of 93 $In_{0.7}Ga_{0.3}As$ NWFETs as a function of NW diameter (d spanning from 14 to 54 nm) clearly shows a monotonic increase of mobility as NW dimension becomes larger. This is possibly due to the enhanced surface scattering in smaller NWs but also the phonon scattering and thermally activated surface/interface traps. Notably, the slope of this function (mobility versus NW diameter) is found to be ~133 $(cm^2 V^{-1}s^{-1})$/nm, which is significantly lower than the reported value of state-of-the-art InAs NWs,[12] suggesting a less sensitive geometrical degradation of mobility for the design consideration of scaled NW transistors.

In order to shed light on the nature of this mobility reduction in smaller NWs, we employ low temperature I-V measurement to further study the diameter dependent behaviors. Figure 4(a) shows the temperature dependent transfer characteristics of a NWFET with a diameter, $d = 40.0$ nm and channel length, $L = 9.9$ μm. It is worth noting that the threshold voltages shift towards the more positive end when temperature lowers, which could be assigned to the less activated surface/interface traps under low temperatures. Moreover, the average mobility of NWs with similar dimension ($d \sim 40$ nm) exhibit a first-rapid increase (from ~4000 to ~6000 $cm^2 V^{-1}s^{-1}$) and then towards saturation behavior (~7500 $cm^2 V^{-1}s^{-1}$) as the temperature lowers from 298 to 77 K as shown in Figure 4(b). This significant mobility enhancement is diminished below 150 K, suggesting that the phonon and surface/interface traps are already frozen out at such low temperature. At the same time, the dependency of mobility on the NW dimension is also investigated at different temperatures, and the data for 11 NWFETs with d = 20 to 40 nm at both 298 and 77 K are presented in Figure 4(c). Specifically, at 77 K where the phonon and traps were illustrated to play insignificant effect in the mobility reduction, there is still a clear monotonic increase of mobility with the NW diameters. Also, impurity scattering should not be a factor here since the NWs are not grown with any intentional doping. As a result, this observed dependency of electron mobility on NW dimension is mainly attributed to

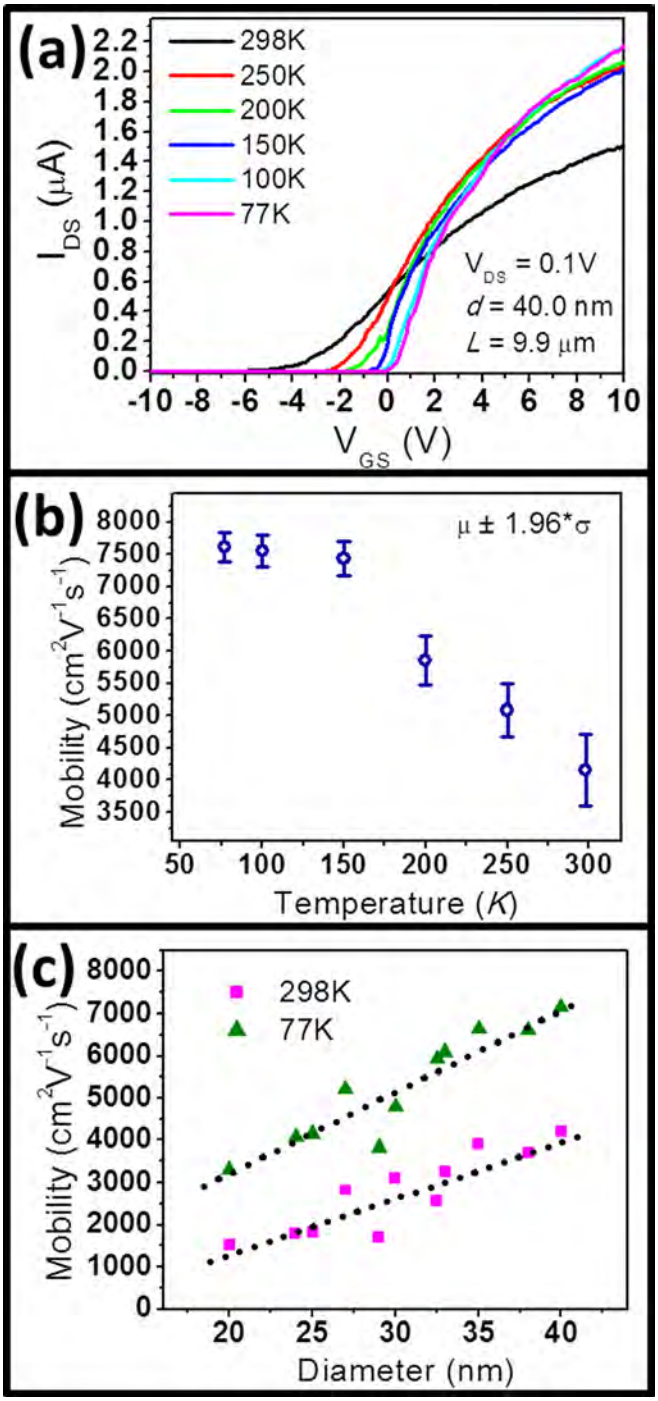

FIG. 4. Temperature-dependent electronic transport characteristics of $In_{0.7}Ga_{0.3}As$ NWFETs. (a) I_{DS}-V_{GS} curve at $V_{DS} = 0.1$ V for a representative NWFET with d = 40.0 nm and L = 9.9 μm over a temperature range of 77-298 K. (b) The corresponding peak field-effect mobility as a function of temperature for the device as shown in (a). (c) Diameter-dependent field-effect mobility for eleven NWs with different diameters measured at temperatures of 77 and 298 K, respectively.

the enhanced surface roughness scattering of electrons in the miniaturized NWs since smaller NWs come with a larger surface-area-to-volume ratio and thus more surface dominating properties. All these can serve as a design guideline in the NW device configuration that aggressive NW channel scaling would accompany with the degradation of the carrier field-effect mobility.

In conclusion, a systematic study of the diameter-dependent electron mobility in InGaAs NWs is presented. The NWs are shown to have good crystallinity and In-rich stoichiometry while the AFM characterization provides a precise estimation of the NW diameter. By exploring the electrical characteristics of the back-gated NWFETs, the peak electron field-effect mobility is found to decrease as the NW diameter reduces. Also, low temperature measurements are performed in order to decouple the effects of surface/interface traps as well as phonon scattering and again confirm that the enhanced surface roughness scattering induces the mobility degradation in miniaturized NWs. This work suggests a careful device design consideration of nanowire dimension is required for achieving the optimal NW device performances.

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