Nanoscale doping of InAs via sulfur monolayers

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One of the challenges for the nanoscale device fabrication of III-V semiconductors is controllable postdeposition doping techniques to create ultrashallow junctions. Here, we demonstrate nanoscale, sulfur doping of InAs planar substrates with high dopant areal dose and uniformity by using a self-limiting monolayer doping approach. From transmission electron microscopy and secondary ion mass spectrometry, a dopant profile abruptness of ~3.5 nm/decade is observed without significant defect density. The n^+/p^+ junctions fabricated by using this doping scheme exhibit negative differential resistance characteristics, further demonstrating the utility of this approach for device fabrication with high electrically active sulfur concentrations of $\sim 8 \times 10^{18}$ cm^{-3}. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3205113]

In recent years, III-V compound semiconductors, such as indium arsenide (InAs), gallium arsenide (GaAs,) and their alloy indium gallium arsenide (InGaAs), have attracted tremendous research and development attention for future active channel materials of metal-oxide-semiconductor field-effect transistors because of their superior electron mobilities.[1–3] However, since the device processing requirements are significantly different from elemental semiconductors such as Si, they impose a major challenge on nanoscale III-V device fabrication.[4,5] Among the many challenges, controlling the postgrowth dopant profiles in III-V compound semiconductors deterministically has not been well addressed. In the silicon (Si) industry, ion implantation has been the dominant doping technique for decades. This process, however, presents problems for compound semiconductors, which consist of two or more chemically and electronically nonequivalent lattice sites. Specifically, the stoichiometry can be altered and difficult to recover from implantation induced crystal damage.[6–8] The residual damage can lead to higher junction leakage and lower dopant activation in compound semiconductors.[9]

Recently, we developed a controllable, nanoscale doping approach for Si substrates by the utilization of molecular monolayers to achieve sub-5-nm ultrashallow junctions (USJs). As opposed to the conventional surface doping techniques, such as solid-source diffusion and spin-on-dopant methods,[10–12] our monolayer doping (MLD) approach provides high areal dose control of the dopants with high uniformity arising from the self-limiting nature of the monolayer formation reaction. Here, we extend the MLD process to compound semiconductors. Specifically, we explore the well-established sulfur (S) monolayer formation on InAs substrates[13–19] to controllably position sulfur dopant atoms on the surface, followed by a subsequent thermal annealing step. As a result, 5 nm S doped junctions are enabled, yielding n^+/p^+ USJs with the diodes exhibiting negative differential resistance (NDR) behavior.

The schematic shown in Fig. 1 illustrates the MLD approach used. First, InAs (001) substrates cleaned with acetone and isopropanol are placed in an ammonium sulfide, $(NH_4)_2S_x$, solution (20% in water, Sigma Aldrich) with excess sulfur (0.2g S per 15 ml of solution). The $(NH_4)_2S_x$ solution is maintained in a water bath at 35 °C. The reaction is performed for 15 min. The InAs substrates are then rinsed in de-ionized water and immediately capped with electron-beam evaporated silicon oxide (SiO_2). Subsequently, thermal annealing from 350 to 450 °C for 300 s is performed to drive in the S atoms to the desired junction depth.

The ammonium sulfide treated surfaces were characterized by x-ray photoelectron spectroscopy (XPS) in an ultrahigh vacuum (~10^{-9} torr) at room temperature with a monochromated aluminum (Al) $K\alpha$ source and pass energy set to 35.75 eV. Figure 2 shows the S $2p$ peak spectra for a monolayer-reacted InAs (001) substrate compared against the signal from a neat (no sulfide treatment) substrate, with the S $2p_{3/2}$ and S $2p_{1/2}$ doublet peak fits. In the monolayer-reacted sample, the S $2p_{3/2}$ peak occurs at 161.6 eV as reported in the literature,[19] with the In $3d$ and As $3d$ peak spectra observed (not shown) closely matching the results

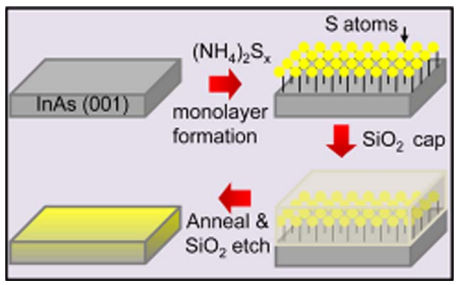

FIG. 1. (Color online) Schematic showing the sulfur monolayer doping approach.

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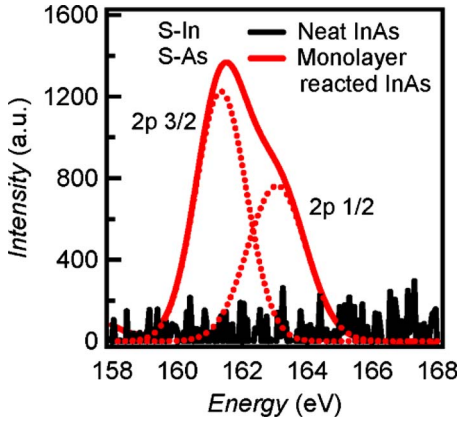

FIG. 2. (Color online) Surface characterization of ammonium sulfide-treated InAs (001) by XPS. The energy range corresponds to the S $2p$ binding energy.

reported by Fukuda *et al.*[19] Because the In–S peak intensity is much stronger than the As–S peak intensity and the binding energies of S to metals lie within the 160–162 eV range, it can be concluded that the S $2p$ peak spectra primarily represents S–In bonding with only minimal S–As bonding present. This is indicative of an InAs surface terminated by an In plane with which the S monolayer is reacted, or the so-called "layer-cake" S-on-In-on-As model. These results are highly consistent with the findings of Petrovykh *et al.*[18] and Fukuda *et al.*[19] suggesting the presence of a S monolayer as the source for our doping technique. The atomic surface density of InAs (001) is 5.6×10^{14} cm^{-2},[20] which represents the maximum areal sulfur dose, assuming a perfect monolayer.

After thermal annealing to drive in the dopants, the InAs/SiO_2 and junction interfaces were investigated by transmission electron microscopy (TEM). The high resolution TEM image for a sample annealed at 450 °C for 300 s depicts the single crystalline nature of the S doped region and the abrupt SiO_2/InAs interface [Figs. 3(a) and 3(b)]. This is in distinct contrast to the number of defects induced

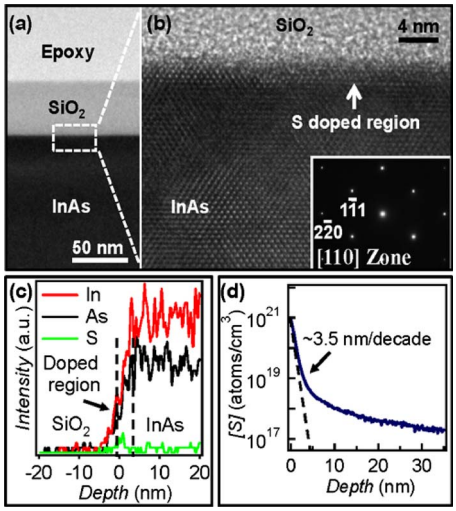

FIG. 3. (Color online) Structural and chemical profiling of S-doped InAs using an annealing condition of 450 °C for 300 s. [(a) and (b)] Low and high resolution TEM images showing SiO_2/S-doped InAs interfaces. The ~4 nm dark contrast region corresponds to the S-doped layer. (c) EDS demonstrating the In, As, and S chemical profiles across the junction interface. (d) SIMS profile of S in InAs. The profile abruptness is ~3.5 nm/decade near the doped surface region.

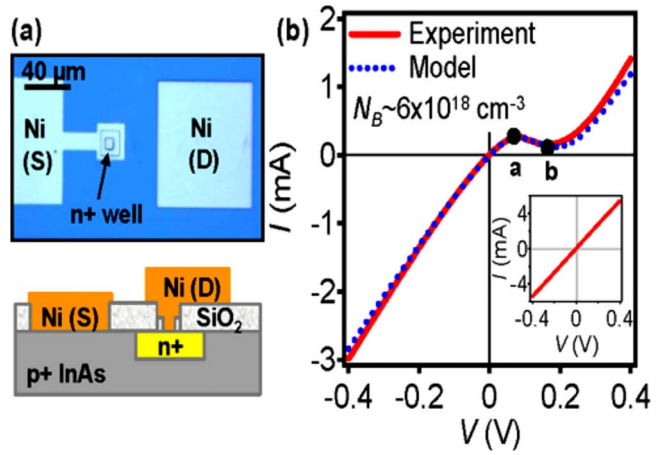

FIG. 4. (Color online) Electrical characterization of diodes enabled by the S-MLD of p^+ InAs substrates ($N_B\sim6\times10^{18}$ cm^{-3}) using an annealing condition of 400 °C for 300 s. (a) Optical image (top) and schematic (bottom) of a representative diode. (b) I-V characteristic of a fabricated diode showing NDR behavior. The junction area is ~314 μm^2. The dashed line shows the modeled I-V curve, assuming a sulfur doping concentration of $N_D=8\times10^{18}$ cm^{-3}. Inset shows the electrical properties of a controlled device, fabricated by the exact procedure, however, without the application of S monolayer.

in conventional ion-implantation techniques. In order to characterize the chemical profile of the junction, energy dispersion spectroscopy (EDS) line profiling was performed across the SiO_2/InAs interface by using scanning TEM mode with a probe size of 0.2 nm, as shown in Fig. 3(c), for which the red, black, and green lines represent the In, As, and S signals respectively. There is a clear S peak at the onset of the In and As signals, indicating the chemical presence of S in the monolayer doped junction. There is ~3.08 at. % of S at ~1 nm from the InAs/SiO_2 interface based on the EDS analysis. The abrupt S profile (~3.5 nm/decade) is further quantitatively confirmed with secondary ion mass spectrometry (SIMS) in Fig. 3(d). A high S concentration of $\sim1\times10^{21}$ cm^{-3}, in agreement with the EDS result, is measured at the InAs surface. This shallow S profile demonstrates the potency of the MLD technique in compound semiconductors for USJ formation.

To examine the electrical properties of the S monolayer doped junctions, n^+/p^+ tunnel diodes were fabricated on heavily Zn-doped InAs substrates ($N_B\sim6\times10^{18}$ cm^{-3}). First, 125 nm of field oxide was deposited on the substrate by electron-beam evaporation. Photolithography and wet etching using 50:1 hydrofluoric acid was used to define the well regions. The sulfur-containing monolayer was then assembled on the exposed InAs well regions and a 35 nm thick SiO_2 cap was subsequently deposited. The sample was annealed in a rapid thermal annealing tool at 400 °C for 300 s, followed by Ni contact (~150 nm thick) formation on top of the sulfur doped regions by defining vias through photolithography and hydrofluoric acid etching [Fig. 4(a)]. Figure 4(b) shows the I-V electrical characteristic of a representative tunnel diode with NDR behavior. For the reverse bias (<0 V), the observed current is due to the band-to-band tunneling as the electrons tunnel from the valence band on the p-side of the junction into the conduction band on the n-side of the junction and the current increases with the bias indefinitely. For forward bias (>0 V), the electrons tunnel from filled states in the conduction band (n^+ side) to unoccupied states in the valence band (p^+ side) to result in a peak

current at point "a" [Fig. 4(b)]. Here the peak voltage $V_p = 0.08$ V and the peak current $I_p = 0.26$ mA. As the forward bias continues to increase, the band overlap diminishes, resulting in the observed NDR. When the *n*-side conduction band edge rises above the *p*-side valence band edge, there are no more states for tunneling resulting in the valley current at point "b" [Fig. 4(b)]. Here, the minimum (valley) voltage, $V_m = 0.16$ V and the minimum (valley) current, $I_m = 0.15$ mA. This gives a peak-to-valley ratio $I_p/I_m = 1.7$, which is a slight improvement over the peak-to-valley ratio of 1.61 reported in the literature obtained by other doping processes for InAs diodes exhibiting NDR behavior.[12] From this onset, normal diffusion current starts to dominate in the forward current. The gamma factor for the diode shown in Fig. 4(b) is $\gamma = (d^2I/dV^2)/(dI/dV) \sim 6.8$, also an improvement over the $\gamma \sim 4.5$ found in the literature.[12] This NDR observation is direct evidence of band-to-band tunneling which requires degenerate doping in both *n*- and *p*-regions with small tunneling barrier width (i.e., abrupt junctions).

Based on Kane's model of tunneling where the electric field is assumed to be constant,[21] the electrically active S concentration is estimated to be $N_D \sim 8 \times 10^{18}$ cm^{-3}, which is close to the highest activated concentration found in the literature.[22] The modeled *I-V* curves based on this doping concentration are shown in Fig. 4, where $n = N_D - N_B$ since the S doping compensates the Zn dopants in the substrate. For the tunnel diode, $N_B = 6 \times 10^{18}$ cm^{-3} and $n = 2 \times 10^{18}$ cm^{-3}. A series resistance of 100 Ω was included in the modeling, which accounts for the parasitic resistance due to the substrate and/or contacts. The modeled tunneling current matches the experimental data fairly closely. The discrepancy between the modeled and SIMS concentration values indicates that only a fraction of the S atoms is electrically active, with the remaining S atoms likely still passivating the surface or occupying nonelectrically active sites in the bulk. The observation of NDR behavior with our monolayer doping approach is a clear indication of heavy S doping with sharp junction abruptness.

Since the surface Fermi level for InAs is known to be pinned at ~0.15 eV above the conduction band,[23,24] control experiments were performed to conclusively demonstrate that the observed NDR behavior of the fabricated diodes is indeed due to S-doping rather than the surface electron inversion layer. In that regard, we fabricated control devices using the exact same fabrication procedure described above and the same p^+ InAs substrate, but without the S monolayer treatment. As a result, the fabricated devices consist of two Ni source/drain contacts formed directly on the p^+ InAs substrate. The *I-V* characteristic of a representative control device is shown in the inset of Fig. 4(b), exhibiting a near-linear behavior attributed to the near Ohmic contact formation to p^+ InAs. This is in contrast to the lightly *p*-doped InAs substrates that are known to be hard to form Ohmic contacts due to the surface inversion layers. However, for the heavily doped p^+ InAs substrates with $N_B \sim 6 \times 10^{18}$ cm^{-3} used in this work, near Ohmic contacts are readily formed by Ni, probably due to the thinning of the tunnel barrier width for such high background dopant concentrations as previously reported.[10] In addition, we fabricated control devices involving S monolayer formation on the surface of p^+ InAs substrate, but without the thermal annealing step to drive in the dopants, followed by Ni contact formation. Once again, the devices showed linear *I-V* characteristics, suggesting the lack of diode formation. The results from the control experiments are in distinct contrast to the S-MLD treated samples that exhibit a clear NDR behavior arising from the heavy *n*-doping of the surface by the thermally diffused S dopants.

Besides the practical implications of the S-MLD approach, our results call into question whether the improvements in the electrical contact behavior observed by "passivating" compound semiconductor surfaces with S monolayers[13,25] is at least partly due to doping the semiconductor as opposed to merely passivating it (i.e., unpinning the Fermi level at the contacts), especially for those experiments where subsequent annealing was used. Furthermore, the reported results show that special consideration of the thermal budget needs to be applied if S passivation is used at the InAs/gate dielectric interfaces, for instance for the atomic layer deposition of gate dielectrics.[26]

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[1] I. J. Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, D. Garcia, P. Majhi, N. Goel, W. Tsai, C. K. Gaspe, M. B. Santos, and J. C. Lee, Appl. Phys. Lett. **92**, 202903 (2008).
[2] Y. Xuan, Y. Q. Wu, and P. D. Ye, IEEE Electron Device Lett. **29**, 294 (2008).
[3] C. Thelander, L. E. Froberg, C. Rehnstedt, L. Samuelson, and L. E. Wernersson, IEEE Electron Device Lett. **29**, 206 (2008).
[4] T. C. Hu, M. F. Chang, N. Weimann, J. Chen, and Y. K. Chen, Appl. Phys. Lett. **86**, 143508 (2005).
[5] S. B. Ogale, Bull. Mater. Sci. **13**, 51 (1990).
[6] N. N. Gerasimenko, G. L. Kuryshev, A. M. Myasnikov, V. I. Obodnikov, L. N. Safronov, and G. S. Khryashchev, Sov. Phys. Semicond., **24**, 785 (1990).
[7] G. I. Kol'tsov, Y. V. Krutenyuk, S. V. Bologov, L. V. Boriskina, A. N. Simonov, and E. A. Frimer, Phys. Chem. Mech. Surf. **2**, 2417 (1985).
[8] P. J. McNally, Radiat. Eff. **6**, 149 (1970).
[9] A. G. Baca, P. C. Chang, A. A. Allerman, and T. J. Drummond, Proc.-Electrochem. Soc. **99**, 155 (1999).
[10] A. V. Lubchenko, A. V. Sukach, S. A. Sypko, Z. F. Ivasiv, V. V. Tetyorkin, and A. T. Voroschenko, Proc. SPIE **4355**, 113 (2001).
[11] H. Khald, H. Mani, and A. Joullie, J. Appl. Phys. **64**, 4768 (1988).
[12] J. B. Hopkins, Solid-State Electron. **13**, 697 (1970).
[13] C. J. Sandroff, R. N. Nottenburg, T. C. Bichoff, and R. Bhat, Appl. Phys. Lett. **51**, 33 (1987).
[14] T. Scimeca, Y. Muramatsu, M. Oshima, H. Oigawa, and Y. Nannichi, Phys. Rev. B **44**, 12927 (1991).
[15] D. Paget, J. E. Bonnet, V. L. Berkovits, P. Chiaradia, and J. Avila, Phys. Rev. B **53**, 4604 (1996).
[16] H. Oigawa, J. F. Fan, Y. Nannichi, H. Sugahara, and M. Oshima, Jpn. J. Appl. Phys., Part 2 **30**, L322 (1991).
[17] D. Y. Petrovykh, J. M. Sullivan, and L. J. Whitman, Surf. Interface Anal. **37**, 989 (2005).
[18] D. Y. Petrovykh, M. J. Yang, and L. J. Whitman, Surf. Sci. **523**, 231 (2003).
[19] Y. Fukuda, Y. Suzuki, N. Sanada, M. Shimomura, and S. Masuda, Phys. Rev. B **56**, 1084 (1997).
[20] M. J. Lowe, T. D. Veal, C. F. McConville, G. R. Bell, S. Tsukamoto, and N. Koguchi, Surf. Sci. **523**, 179 (2003).
[21] E. O. Kane, J. Appl. Phys. **32**, 83 (1961).
[22] V. N. Morozov and V. G. Chernov, Sov. Phys. J. **24**, 506 (1981).
[23] N. Li, E. S. Harmon, J. Hyland, D. B. Salzman, T. P. Ma, Y. Xuan, and P. D. Ye, Appl. Phys. Lett. **92**, 143507 (2008).
[24] H. H. Wieder, J. Vac. Sci. Technol. B, **21**, 1915 (2003).
[25] G. Eftekhari, Vacuum **67**, 81 (2002).
[26] F. S. Aguirre-Tostado, M. Milojevic, K. J. Choi, H. C. Kim, C. L. Hinkle, E. M. Vogel, J. Kim, T. Yang, Y. Xuan, P. D. Ye, and R. M. Wallace, Appl. Phys. Lett. **93**, 061907 (2008).