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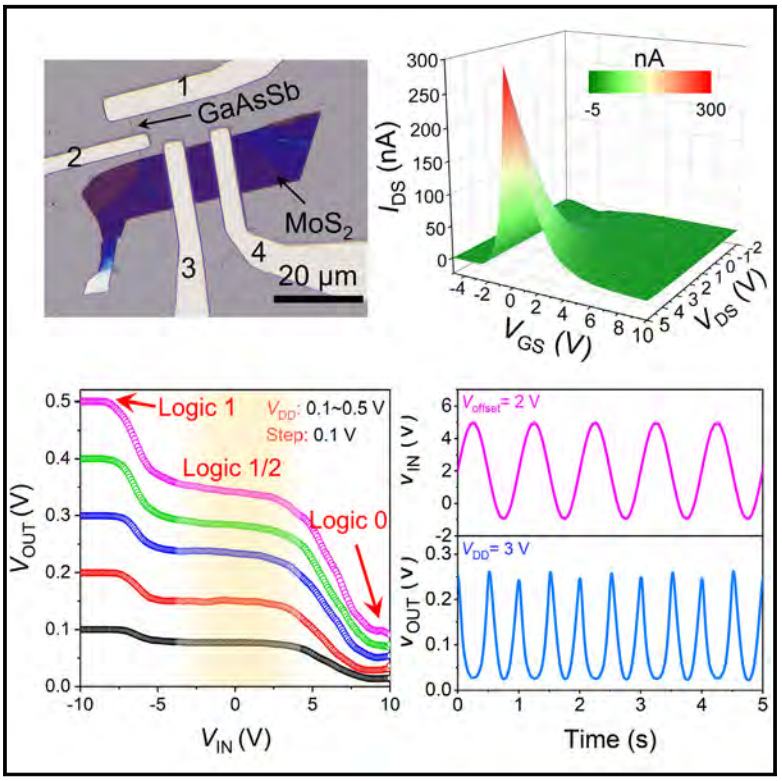
Multifunctional anti-ambipolar electronics enabled by mixed-dimensional 1D GaAsSb/2D MoS_2 heterotransistors

Graphical abstract



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In brief

The mixed-dimensional anti-ambipolar transistor can be realized based on the 1D GaAsSb/2D MoS_2 van der Waals heterojunction, enabling the implementation of multifunctional logic circuits and thus simplifying the integrated circuit design. The reduced active area of the heterostructures can effectively restrain the limited frequency characteristics. Integrated with a p-GaAsSb FET or an n-MoS_2 FET, the anti-ambipolar transistor can function well as a ternary logic inverter and a frequency multiplier, respectively.

Highlights

- Designed the multifunctional 1D/2D anti-ambipolar heterotransistors
- Realized highly confined 1D active region of heterojunctions
- Accounted for the mechanism of anti-ambipolarity with a high peak-to-valley ratio
- Demonstrated the multivalued logic circuit and frequency multiplier synchronously

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Multifunctional anti-ambipolar electronics enabled by mixed-dimensional 1D GaAsSb/2D MoS_2 heterotransistors

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THE BIGGER PICTURE The geometric scaling of transistors has gradually hit a plateau in recent years, along with the stubbornly high fabrication cost. Besides, the long-standing issues of increasing leakage current and wiring density accompanied by the device miniaturization have an adverse impact on power consumption. Aided by the introduction of anti-ambipolar transistors, the versatility in multivalued logic and analog circuits can be implemented, projecting a massive revolution in chip circuit design with higher information processing capacity and reduced power consumption. While recent studies have shown the capability of realizing ternary logic inverters based on anti-ambipolar transistors, the frequency characteristic and energy efficiency are rarely explored, restricting their practical applications in logic circuits and optoelectronics. In this work, we design and demonstrate an anti-ambipolar device with active region downscaling, thus realizing high-performance logic and analog circuits.

SUMMARY

The incapability of effective multifunctional logic operations for most reported heterostructure electronic devices has impeded further simplification of the prevailing complex integrated circuit design. Here, an anti-ambipolar transistor is successfully demonstrated based on a mixed-dimensional GaAsSb nanowire/MoS_2 nanoflake heterojunction. Due to the strong interfacial coupling and band-structure alignment properties, the prominent anti-ambipolar transfer characteristics with the flipping of transconductance are readily achieved, showing a high peak-to-valley ratio of over 10^3 on either side of the peak current. The anti-ambipolar transistor is then leveraged to perform the multivalued inverter with low supply voltage. Furthermore, the frequency doubling circuits are explored by exploiting the flipping of transconductance of the heterotransistor. The output voltage of the frequency multiplier oscillates at a 2-fold frequency in response to the input analog circuit signal. The mixed-dimensional anti-ambipolar transistors developed in this study are a step toward next-generation multifunctional integrated circuits and telecommunication technologies.

INTRODUCTION

Device downscaling has driven integrated circuit technology advancements in the semiconductor industry over the last decades.[1] However, complementary metal-oxide-semiconductor (CMOS) scaling has started reaching its physical and economic limits at the sub-10-nm technology node, which brings an enormous challenge to fabricating the nanoscale devices in a controllable and cost-effective manner.[2–4] Further scaling of transistor size would increase leakage current and, hence, excessive power dissipation.[5] To tackle this issue, various technological innovations have proceeded toward developing energy-efficient device architectures with area reduction. In order to enhance the electrostatic gate control on the channel and thus diminish the punch-through effect, different device architectures, including silicon-on-insulator structures,[6,7] fin field-effect transistors (FinFETs),[8,9] and gate-all-around devices,[10,11] have been proposed. Nevertheless, more than 90% of the total power consumption for highly scaled chips can be attributed to the enormous wiring network used for clock distribution. Thus, the

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progressive improvement in device architecture alone would not be appropriate due to the significant rise in power consumption.[12] This calls for an alternative technology to settle the encountered bottleneck problem circuitously. Given this setting, the advent of multivalued logic (MVL) is considered a promising way to overcome the increasing power consumption.[13–15] Due to the characteristics of multivalued logic states, MVL can enable higher information density than the conventional binary Boolean logic. Then the logic functions can be performed with fewer logic gates and interconnect, simplifying the sophisticated wiring network and reducing the chip power consumption and RC delays.[16–18] For example, the transition from binary to ternary logic is estimated to dramatically reduce the system complexity by up to 63% of the original level.[19] In this regard, MVL possesses application prospects in the augmentation of binary systems, arithmetic, memory, and signaling.[20]

To date, significant efforts have been devoted to constructing various MVL gates by devising compact unit devices suitable for MVL systems. This way, the emergence of the unit device with multiple threshold voltages has been demonstrated as an effective strategy for high-density information processing without increasing the circuit complexity.[21–23] Thereinto, the most typical device architectures include anti-ambipolar transistors (AATs),[24,25] zero differential transconductance devices,[26,27] and negative differential resistance devices.[28,29] It is worth mentioning that the anti-ambipolarity of AAT is quite advantageous to the development of multifunctional devices in optoelectronics, MVL circuits, and telecommunication technologies due to the feature of transconductance flipping, which makes it become the most widely explored class of MVL devices.[30,31] For instance, the tunable ternary inverter via the integration of BP/MoS_2 van der Waals (vdW) AAT and 0*p*-type FET was successfully achieved with distinct multi-logic states.[14] In addition, the binary frequency shift keying was implemented by exploiting the anti-ambipolar single-walled carbon nanotube (SWCNT)/amorphous indium gallium zinc oxide (α-IGZO) heterostructure devices as well.[32] However, almost all the AAT-based devices are configured either by 2D vdW materials or organics. The instability of organics and large V_{DD} values of over 10 V restrict the deployment of these organic MVL devices for large-scale semiconductor device integration.[33] Moreover, the frequency characteristic of these MVL devices and the function of frequency doubling are less tested and reported due to the relatively large active region. The high operating frequency of MVL and frequency doubling circuits demands the shrinking of the device dimensionality, for downscaling the active region can reduce the junction capacitance and thus render the devices intrinsically faster and energy efficient.[32,34] As a result, the mixed-dimensional heterostructures consisting of 1D nanowires (NWs) and 2D vdW semiconductor materials could refrain from the drawbacks of limited frequency characteristic and high energy consumption, thus realizing the high-performance versatile MVL circuits. On the one hand, the reduced dimensionality of nanowires can efficaciously scale down the active region of the heterostructures. On the other hand, the nature of dangling-bond-free surface of 2D materials can give rise to the strong vdW coupling effect in such mixed-dimensional heterostructures, leading to the efficient charge transport at the heterointerface. Therefore, the synergistic effect in the mixed-dimensional heterostructures would bring great scientific significance in constructing AATs with versatile logic circuit functionalities.

Herein, we developed an AAT device based on 1D *p*-type GaAsSb/2D *n*-type MoS_2 heterojunctions, whereby the multifunctionality of MVL and frequency doubling was demonstrated synchronously for the first time in this research. Through stoichiometric variation, the multi-element feature of ternary GaAsSb allows the modulation of electronic properties and band alignment with MoS_2 nanoflake. Owing to the strongly coupled heterointerface and high intrinsic carrier mobility of both constituents, the developed mixed-dimensional heterojunctions present pronounced anti-ambipolarity and gate-tunable rectifying behavior. More importantly, by engineering the partition load, a multivalued inverter exhibiting three true logic states was achieved based on the GaAsSb/MoS_2 AAT device. Besides, anti-ambipolarity also facilitates the realization of analog signal processing, like frequency multipliers. In light of this, the frequency doubling performance was evaluated using the GaAsSb/MoS_2 AAT unit device. As a result, the frequency of output voltage on the loading resistance doubled relative to the input signal. These high-performance devices herald the technological potential of the mixed-dimensional GaAsSb/MoS_2 anti-ambipolar heterojunction for future versatile electronics.

RESULTS

Comparison of GaAsSb/MoS_2 in-series FET and AAT

In order to achieve the desired GaAsSb/MoS_2 anti-ambipolar heterotransistors, the GaAsSb NWs require to be synthesized with high crystallinity and respectable electrical properties. As demonstrated in Figure S1 and Note S1, high-quality GaAsSb NWs were fabricated through the recently developed thiourea-assisted solid-source chemical vapor deposition (SS-CVD) technique, as reported elsewhere.[35] Excellent electrical properties are also confirmed by evaluating the device performance of NW FET, binary CMOS inverter, and PMOS resistor inverter on GaAsSb NW (Figures S2–S7 and Notes S2–S7). The well-functioned inverters presented here manifest the great potency of the GaAsSb NWs for high-performance AAT devices and logic circuits.

To achieve the reliable anti-ambipolarity for subsequent applications in logic circuits, two different types of device configurations based on GaAsSb NW and MoS_2 nanoflake were assembled and compared. Minimal power consumption could be accomplished by reducing the supply voltage V_{DD}. For instance, the supply voltage of state-of-the-art carbon nanotube 5-nm node FET is around 0.4 V.[36] Hence, the V_{DD} values are set to be lower than 1.0 V to reduce the total device power consumption for comparison. The schematic of the in-series FETs and the corresponding equivalent circuit diagram are shown in Figures 1A and 1B, respectively. By joining the GaAsSb and MoS_2 FETs in series, the anti-ambipolar characteristic arises in a device structure with either positive or negative drain biases (Figure 1C). The anti-ambipolarity of the in-series FETs is evidently dictated by both *p*- and *n*-type components. In comparison, the GaAsSb/MoS_2 AAT is composed of three components in a series-resistance mode: *n*-type MoS_2 FET, GaAsSb/MoS_2 *p*-*n* junction,

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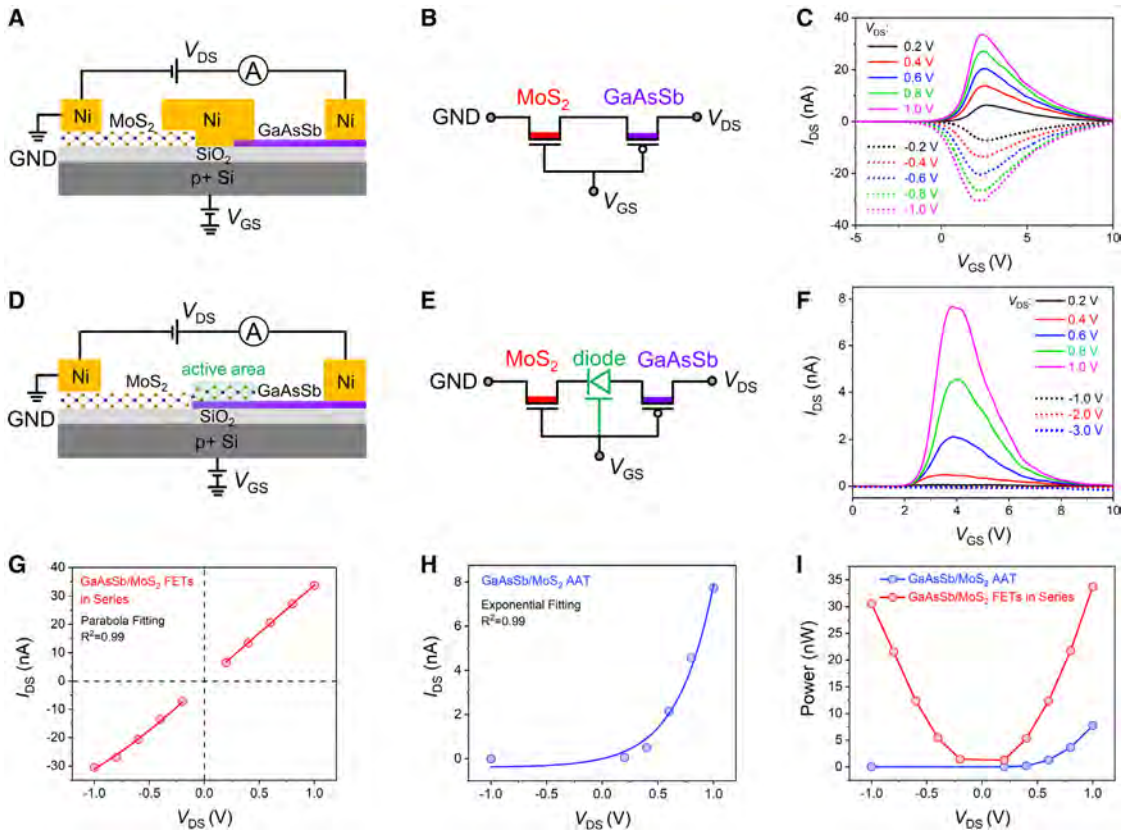

Figure 1. Electrical properties of GaAsSb/MoS_2 FETs in series and GaAsSb/MoS_2 AAT

(A and D) Schematics of the devices configured by the GaAsSb and MoS_2 in-series FET and AAT, respectively.

(B and E) Corresponding equivalent circuit diagrams of (A) and (D).

(C and F) Transfer characteristics of the GaAsSb/MoS_2 in-series FET and AAT with positive and negative V_{DS} voltages. Comparison of (G and H) I_{peak}-V_{ds} plots and (I) power consumption for GaAsSb/MoS_2 in-series FET and AAT, respectively.

and *p*-type GaAsSb FET, as shown in Figures 1D and 1E. The mixed-dimensional AAT device exhibits typical anti-ambipolar transfer characteristics, as shown in Figure 1F. Due to the existence of space charge region (SCR) lying in the stacked GaAsSb/MoS_2 heterojunction, the channel peak current is much lower in the AAT device than the in-series FETs, although both the device sizes are similar in terms of the channel length, width, and thickness. Besides, the channel current of the AAT remains at minus picoampere level under reverse biases, indicating the apparent rectifying behavior in the AAT device. By contrast, the transfer curves of the in-series FETs are nearly symmetric at ± V_{DS}, which could be further validated by the linear output plots in Figure S8. The peak current values at varying V_{DS} for GaAsSb/MoS_2 AAT and in-series FETs are extracted from the transfer curves in Figures 1C and 1F, respectively. As displayed in Figures 1G and 1H, the I_{peak}-V_{DS} plots are well fitted to the parabolic and exponential expressions for the in-series FETs and AAT, respectively.[37–39] The I_{peak} almost increases linearly with the increase of V_{DS} for the in-series FETs. At the same time, it witnesses an exponential upward trend with drain bias for the AAT device, which is in accordance with the diode characteristics. Then the power consumption at the current maximum is calculated according to the formula $P = I_{DS} \times V_{DS}$, which is demonstrated in Figure 1I. Despite the analogous device size as AAT, the in-series FETs are subjected to relatively high power consumption. Moreover, although the device configured by GaAsSb/MoS_2 FETs in series also behaves with obvious anti-ambipolarity, the complicated architecture with more metal interconnects makes it inferior to the compact three-terminal AAT device. So, the emerging AAT devices based on the heterojunction structures outperform the in-series FETs regarding wiring density and power consumption. Based on the above analysis results, the subsequent study will focus on appraising AAT devices' electrical properties and associated applications in logic and analog circuits.

Electrical characteristics of the GaAsSb/MoS_2 AAT

The lateral GaAsSb/MoS_2 heterojunction AAT device was prepared by stacking a MoS_2 nanoflake above the GaAsSb NW on a 50-nm SiO_2/Si substrate. Two pairs of Ni electrodes were separately positioned on the constituent semiconducting materials, away from the overlapped junction area, as presented in the optical microphotograph in Figure 2A. The linear relationship of I_{DS}-V_{DS} curves indicates that both GaAsSb and MoS_2 are well

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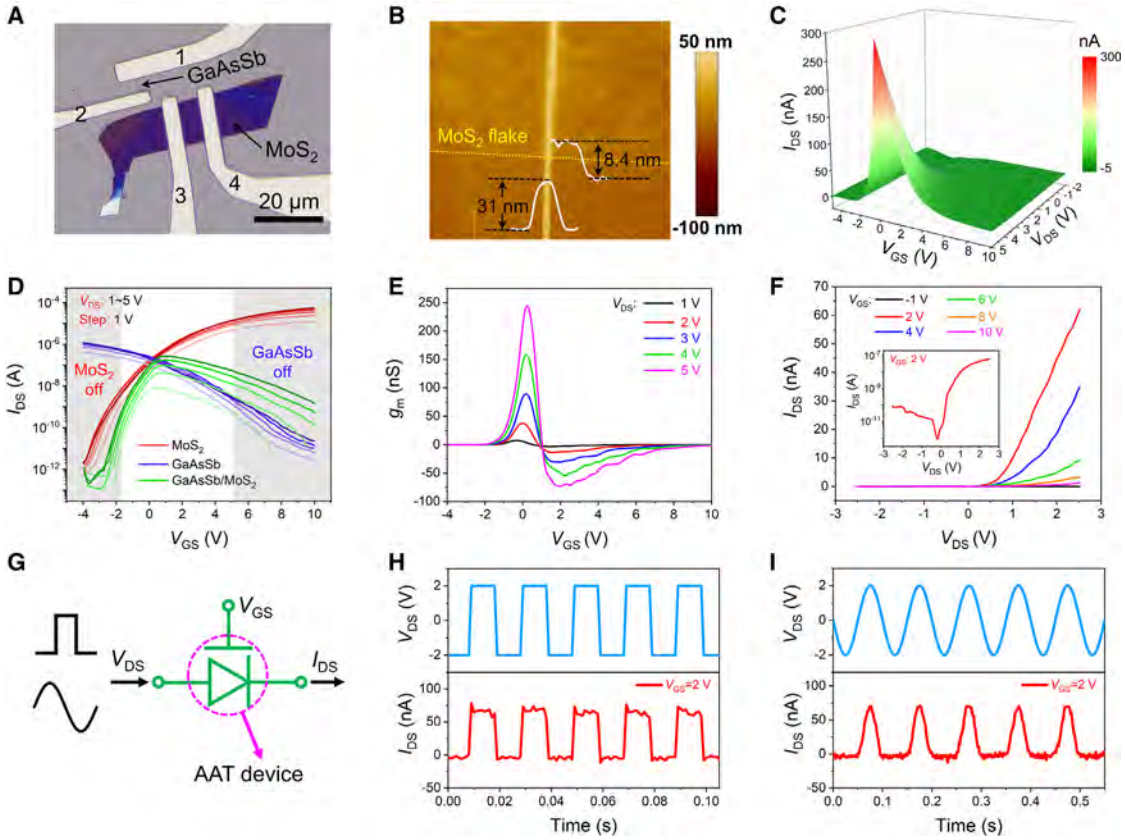

Figure 2. Electrical performance of the GaAsSb/MoS_2 heterojunction AAT device

(A) Optical microphotograph of a typically stacked GaAsSb/MoS_2 heterojunction device on the 50-nm SiO_2/Si substrate.

(B) AFM image of the GaAsSb/MoS_2 heterostructure in (A).

(C) Three-dimensional representation of output characteristics of the GaAsSb/MoS_2 heterotransistor at varying gate biases.

(D) Semilog transfer characteristics of the *p*-type GaAsSb FET (blue), *n*-type MoS_2 FET (red), and GaAsSb/MoS_2 AAT device (green) in (A).

(E) Corresponding transconductance calculation of the GaAsSb/MoS_2 AAT device in (D) at different V_{DS}.

(F) Gate-tunable output characteristics of the GaAsSb/MoS_2 AAT device. The inset shows the semilog I_{DS}-V_{DS} curve of the device under gate bias of 2 V.

(G) Schematic of the rectifying behavior measurement of the AAT device circuit under applied AC source-drain bias.

(H and I) Measurement results of the rectified output current of the AAT device under input AC voltage of (H) square waveform at 50 Hz and (I) sinusoidal waveform at 10 Hz.

contacted with Ni electrodes (Figures S4E and S4F), ensuring efficient hole and electron injection, respectively.[35,40] The detailed fabrication process for the AAT device can be found in the experimental procedures section. The transport channel between electrodes 2 and 3 constitutes a typical GaAsSb/MoS_2 heterotransistor, which is the combination of a *p*-type GaAsSb FET, a GaAsSb/MoS_2 heterojunction, and an *n*-type MoS_2 FET in series. The thicknesses of the GaAsSb NW and MoS_2 nanoflake are confirmed by atomic force microscopy (AFM) to be about 31 nm and 8.4 nm, respectively (Figure 2B). This device structure enables electrical characterization of the GaAsSb/MoS_2 heterotransistor through the global gate controlling the electrostatic potential of the channel. Figure 2C shows a three-dimensional plot of output characteristics (I_{DS}-V_{DS}) at varying gate biases with *n*-contact (electrode 3) grounded. Due to the non-uniformity of the channel constitution, the source-drain current exhibits apparently anti-ambipolar characteristics under gate modulation.[41,42] Concretely, the conductance of the heterotransistor device reaches its maximum at near V_{GS} = 0 V and decreases on varying the gate bias in either polarity. The transfer plots in Figure 2D can further demonstrate the gate tunability of the current through the heterotransistor channel. The anti-ambipolarity of the heterotransistor (transfer curve in green) can be qualitatively viewed as a superposition of the *p*-type GaAsSb (purple) and *n*-type MoS_2 (red) FET transfer characteristics. Specifically, the total current of the AAT peaks when both GaAsSb and MoS_2 transistors are turned on (0 V < V_{GS} < 2 V) and declines to a minimum when either device is turned off (V_{GS} = −4 V or 10 V). It is worth mentioning that the negligible hysteresis from 10 consecutive double-sweep I_{DS}-V_{GS} curves of the GaAsSb/MoS_2 AAT (Figure S9) is probably caused by the crystal lattice defects in the MoS_2 nanoflake, dielectric layer, etc.

Meanwhile, peak-to-valley ratio (PVR), defined as the ratio of peak/on current and valley/off current, is an important performance metric for an anti-ambipolar device. A high PVR is desirable to implement the ternary logic circuit with the fast logic state

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transition. Meanwhile, a low off current can effectively restrain power consumption. It can be seen from the transport plot that the PVR exceeds 10^3 for both GaAsSb and MoS_2 sides, suggesting the mixed-dimensional AAT device is suitable for advanced logic applications.[32,43] It is noted that the anti-ambipolar pattern of the GaAsSb/MoS_2 AAT transfer plot is asymmetric, with different slopes on either side of the I_{DS} peak. This could be further evidenced by the transconductance calculation results in Figure 2E. The asymmetric anti-ambipolarity has tremendous potential advantages in the field of communications and can be harnessed to build phase and amplitude shift keying units.[32,42]

The output characteristics of the mixed-dimensional AAT with varying gate biases are shown in Figure 2F. It is clear that the diode-like rectifying behavior and rectification ratio can be consecutively tuned by gating (Figure S10). Well-behaved rectifying behavior is achieved along with a high rectification ratio of up to 10^3 at V_{GS} = 2 V (Figure 2F inset). However, the rectifying behaviors degenerate when V_{GS} is larger or smaller than 2 V, ascribed to the gradual exhaustion of carriers in the *p*/*n*-type channel.[44] As confirmed in Figures S4E and S4F, the good contact of both GaAsSb and MoS_2 with Ni has a negligible effect on the diode characteristics. Therefore, the electrostatic gating effect is verified to be capable of simultaneously tailoring the unintentional doping of both semiconductors in the channel, thereby allowing tunability in the built-in voltage and rectifying behavior of the AAT device. Moreover, dynamic rectification measurement of the AAT device was carried out under square and sinusoidal alternating current (AC) pulses, as schematically shown in Figure 2G. At V_{GS} = 2 V, apparent dynamic rectifying behaviors are observed from the time domain current plot under 50-Hz square AC pulse (V_{DS} = ±2 V) in Figure 2H. The dynamic current at V_{DS} = 2 V is the same as the static value observed in Figure 2F. Another rectification dynamics was taken with 10-Hz sinusoidal AC pulses (Figure 2I). No obvious time delay is observed from either of the dynamic current plots, implying that the AAT device can convert AC to direct current (DC) without phase lag. The distinct anti-ambipolarity of more GaAsSb/MoS_2 heterotransistors with the same architecture can be found in Figures S11 and S12. It can be seen that the peak current level, peak position, and width of the on-state region can be correspondingly modulated by controlling the device size and carrier density of the AAT components.

Heterointerface quality and energy band alignment

Next, the origin of the apparent anti-ambipolarity and gate-tunable rectifying behavior was probed from the perspective of the heterointerface quality of the GaAsSb/MoS_2 AAT device. The Raman and micro-photoluminescence (μ-PL) measurements were carried out by a 532-nm laser source with a spot diameter of ~1 μm. Raman spectra collected from the individual materials and the overlap region of the heterostructure are exhibited in Figure 3A. The observed Raman peaks of MoS_2 at 384 cm^{-1} and 408 cm^{-1} correspond to the in-plane (E^1_{2g}) and out-of-plane (A_{1g}) vibrational modes, as reported previously.[45] The Raman spectrum for GaAsSb includes three prominent peaks at 227 cm^{-1}, 239 cm^{-1}, and 243 cm^{-1} (Figure S13A), which are attributed to the GaAs-like TO, GaSb-like LO, and GaAs-like TO phonon modes, respectively.[46] Characteristic peaks corresponding to both constituting materials are notably observed in the overlap region, confirming the formation of the GaAsSb/MoS_2 heterostructure. Compared with the individual MoS_2, the Raman intensity of the overlap region is apparently quenched, as shown in Figure S13B, indicating the strong interfacial coupling in the mixed-dimensional heterojunction.[47,48] The Raman mapping of MoS_2 at 384 cm^{-1} (Figure 3B) and GaAsSb at 227 cm^{-1} (Figure S13C) further verifies the high quality of the heterostructure, which benefits the efficient carrier transport across the heterointerface. Subsequently, the polarized Raman scattering measurements were conducted for the single GaAsSb NW and GaAsSb/MoS_2 overlap region (Figure S14). Although the NW lies underneath the MoS_2 nanoflake at the heterojunction, both the GaAsSb NW and overlap region exhibit correlated 90° periodicity of Raman intensity, which is related to the selection rules for one-dimensional geometry of zinc blende semiconductors.[49,50] To examine the optical properties, μ-PL was performed on the GaAsSb/MoS_2 heterostructure. The laser was selectively focused on individual MoS_2, and GaAsSb/MoS_2 overlap regions. A similar PL quenching effect can also be observed at the heterojunction area (Figures 3C and S13D). It signifies the efficient separation and transition of photogenerated carriers occurred at the heterointerface, leading to the increase of nonradiative recombination and, thus, the quenched PL emission. The pronounced interfacial coupling effect proved above would be vital in constructing high-performance and multifunctional electronics.

After verifying the high-quality heterointerface of the AAT, the band alignment of the GaAsSb/MoS_2 AAT device is schematized to understand the operation mechanisms better. Upon contact, the two semiconductors would form a typical type-II *p*-*n* heterojunction, as reported elsewhere.[30] As mentioned above, the anti-ambipolarity of this AAT device is a synthetical result of three functional parts connected in series: *p*-type GaAsSb FET, GaAsSb/MoS_2 *p*-*n* diode, and *n*-type MoS_2 FET. In Figures 3D–3F, $V_{th,n}$, and $V_{th,p}$ denote the threshold voltages of MoS_2 FET and GaAsSb FET, respectively. The gate is used to tune the doping concentration of both semiconductors. When V_{GS} is lower than $V_{th,n}$ of the MoS_2 FET (Figure 3E) or higher than $V_{th,p}$ of the GaAsSb FET (Figure 3F), the *n*- or *p*-type channel of the AAT device is considerably depleted. In the case of the band diagram, this corresponds to a significant pushdown or pushup at the Fermi level. Then the device is doped as a p^+-*i* or *i*-n^+ junction, leading to low conductance of the series-connected AAT device. Likewise, the forward diode current can only flow through the AAT device channel when both the MoS_2 FET and GaAsSb FET are turned on, i.e., $V_{th,n} < V_{GS} < V_{th,p}$ (Figure 3D). Next, the band diagram evolution of the AAT device under various drain biases at on-state ($V_{th,n} < V_{GS} < V_{th,p}$) is shown in Figures 3G–3I. Under reverse bias (Figure 3G), the energy barrier for the carriers in both semiconductors is increased. The electrons in MoS_2 (holes in GaAsSb) cannot overcome the barrier in the conduction (valence) band, resulting in a minimal reverse current. With a forward bias applied (Figure 3H), the potential barrier and SCR will be diminished. Concomitantly, the energy band of the GaAsSb side and MoS_2 side will also be pulled down and up, respectively. In this way, the offset of the conduction band is negligible for the transport of electrons in MoS_2, for the peak barrier is covered by

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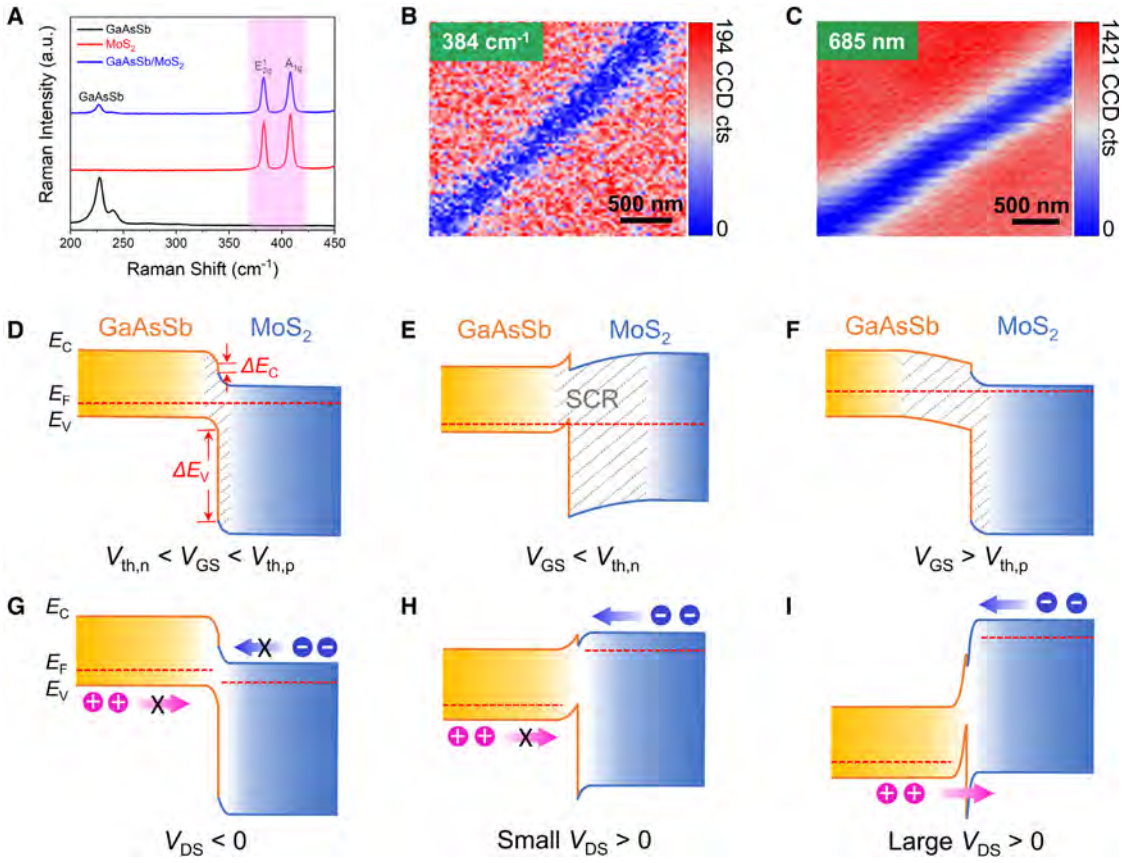

Figure 3. GaAsSb/MoS_2 heterointerface quality and band diagram evolution

(A) Raman spectra of the individual GaAsSb NW, MoS_2 nanoflake, and GaAsSb/MoS_2 heterostructure.

(B) Raman mapping image for the GaAsSb/MoS_2 heterostructure at the wavenumber of 384 cm^{-1}.

(C) PL mapping was measured at the wavelength of 685 nm on the GaAsSb/MoS_2 heterostructure.

(D–F) Schematic of the energy band structure of the GaAsSb/MoS_2 AAT device at an equilibrium state when (D) $V_{th,n} < V_{GS} < V_{th,p}$, (E) $V_{GS} < V_{th,n}$, and (F) $V_{GS} > V_{th,p}$.

(G–I) Energy band diagrams of the on-state GaAsSb/MoS_2 AAT device ($V_{th,n} < V_{GS} < V_{th,p}$) at different V_{DS} bias conditions.

the steep band structure. But the barrier for holes in GaAsSb is still large when V_{DS} is small. When V_{DS} increases further until the valence band of GaAsSb is pulled down beyond the valence band position of MoS_2 (Figure 3I), the holes in GaAsSb can tunnel through the narrow peak barrier under a large forward bias. The current transport of the AAT device is then dominated by both GaAsSb and MoS_2 channels. The larger the drain bias is, the more effectively the gate field controls the AAT channel, where no internal barrier exists to restrain carrier transport. This observation explains the small on-state current when $V_{DS} \leq 1$ V (Figure 1F) and a sharp rise in current as V_{DS} increases, as shown in Figure 2D.

Multivalued logic inverter

Due to the significant superiority of multiple logic states, MVL devices are expected to provide higher data storage density as well as data processing efficiency than binary logic circuits.[14,24] Herein, as a fundamental building block in MVL applications, a ternary inverter was demonstrated using the AAT with the feature of sign-changing transconductance. This inverter, as schematically depicted in Figure 4A, is formed by the integration of the GaAsSb/MoS_2 heterostructure AAT as a driver (pull-down transistor) with the built-in GaAsSb *p*-type NW FET as a load resistor (pull-up transistor) on a 50-nm SiO_2/Si substrate. Figure 4B shows the equivalent circuit diagram of the fabricated ternary inverter. The supply (V_{DD}) and input voltages (V_{IN}) were applied to the source contact of the GaAsSb NW FET and Si back gate, respectively. The source contact in the GaAsSb/MoS_2 AAT was grounded (V_{SS}), and the output voltage (V_{OUT}) was measured on the common drain contact for both GaAsSb NW FET and GaAsSb/MoS_2 AAT. The V_{OUT} of the ternary inverter is determined by the resistance ratio between the two devices in series, i.e., the AAT and GaAsSb FET, which can be modulated by the back gate (V_{IN}).

In order to gain an insight into the resistance ratio, the transfer characteristics of the two devices forming the inverter were first assessed. As shown in Figure 4C, the AAT and GaAsSb FET deliver typical anti-ambipolar and *p*-type unipolar semiconducting behaviors, respectively. Meanwhile, it is noticeable that the transfer curves can be divided into three V_{IN} ranges, as marked

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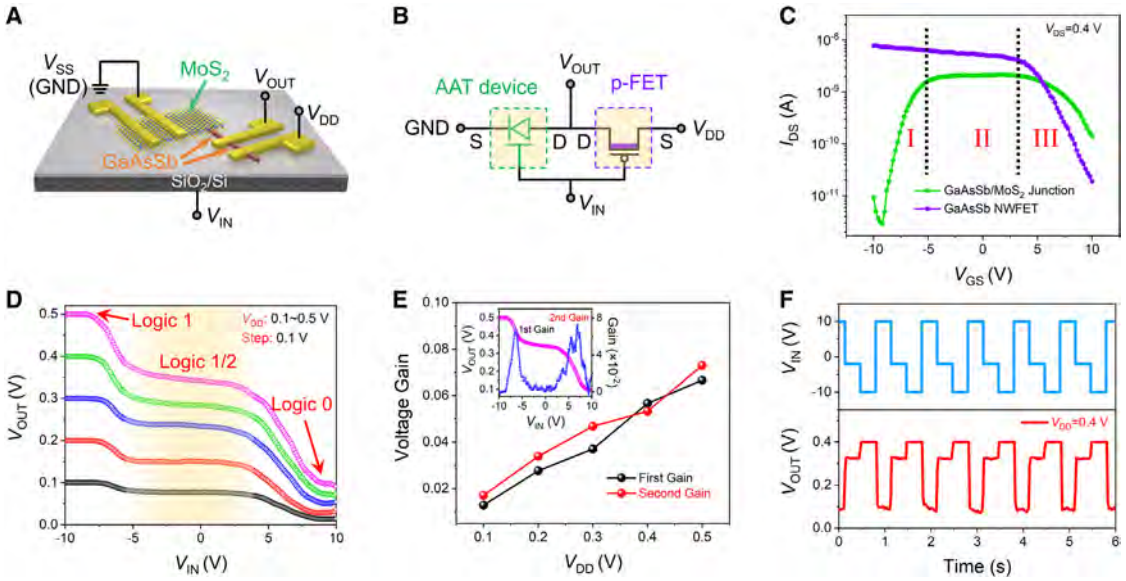

Figure 4. Ternary logic inverter integrated by the GaAsSb FET and GaAsSb/MoS_2 AAT device

(A) Device schematic of the GaAsSb/MoS_2 heterojunction-based ternary inverter.

(B) Equivalent circuit diagram of the ternary logic inverter.

(C) Semilog transfer characteristics of a *p*-type GaAsSb FET (blue, V_{DS} = 0.4 V) and GaAsSb/MoS_2 AAT device (green, V_{DS} = 0.4 V).

(D) Voltage transfer characteristics of the GaAsSb/MoS_2 heterojunction-based ternary inverter at different V_{DD} values.

(E) Corresponding voltage gain of both switching states of the inverter at different V_{DD} values. Inset: typical voltage gain dependence of V_{IN}.

(F) Transient plots of output voltages of different logic states in response to applied input voltages of 1 Hz.

in Figure 4C. In range I ($V_{IN} < -5$ V), the drain current of GaAsSb FET is much higher than that of the AAT, for the *n*-type constitution in AAT is fully turned off. In range II (-5 V < V_{IN} < 3 V), both the AAT and *p*-FET are turned on with effective gate control, and a long approximately parallel region exists for the two transfer plots. While in range III (3 V < V_{IN}), a further increase in V_{IN} renders the drain current variation opposite to the situation in the range I because of the exhausted carriers in GaAsSb FET. In this way, the V_{IN}-induced variations in drain current through the AAT and *p*-FET channels would then produce three main different resistance ratios. Consequently, three distinct logic states explicitly emerge in the voltage transfer characteristics (VTCs) of the ternary inverter at different V_{DD} (Figure 4D). In detail, at logic 1, the GaAsSb FET in the pull-up network would provide a low resistive path to the supply voltage that yields a high output voltage close to V_{DD}. On the contrary, the resistance of the AAT channel in the pull-down network is far smaller than the *p*-FET at logic 0, thus rendering the logic low level nearly equal to GND. As discussed earlier, the parallel region of the AAT and *p*-FET in the semilog transfer characteristics indicates that the resistance ratio between the pull-up and pull-down transistors is nearly constant. Then, a unique intermediate logic state (logic 1/2) comes into being in the VTC at varying V_{DD}. Interestingly, the middle logic state will appear even at a small V_{DD} of 0.1 V, surpassing the reported MVL inverters in other studies[14,16,51] where the middle logic state would not appear until relatively large V_{DD} values are supplied.

As one of the most crucial figure of merits of a ternary inverter, the width of the middle-state plateau can appraise the tolerance window and stability of the mid-state. When V_{DD} increases from 0.1 to 0.5 V, the middle logic region keeps quite flat with few fluctuations, along with a large V_{IN} window of ~8 V, suggesting the robustness and stability of the MVL device operations. The extracted output voltages in respective logic states from the VTC are compiled in Table S1, showing clear margins of transition between various logic levels. Figure 4E presents the corresponding voltage gains of this ternary inverter at different V_{DD} values. Both voltage gains witness an upward trend with the increase of V_{DD}. Figure 4F displays the dynamic switching property of the ternary inverter at a V_{DD} of 0.4 V. Three different V_{IN} values (10 V, -2 V, and -10 V) are applied at a frequency of 1 Hz. As a result, this inverter exhibits no notable hysteresis regardless of the V_{IN} evolvement, indicating stable ternary operation of this inverter device. The MVL behavior of another ternary inverter with the same device configuration can be found in Figure S15. With the implementation of device geometry optimization, for instance, exploiting a top-gated structure with high-κ dielectric, it is promising to enhance the logic device performance further.

Here, the distinctive aspect in the implementation of MVL circuits is that the ternary inverter is constructed by the unipolar GaAsSb *p*-FET in our research. In general, however, the ambipolar transistors, such as $MoTe_2$ FETs, BP FETs, and organic PTCDI-C8 FETs, are employed as the *p*-FETs in multivalued logic circuits.[14,25,33] On the one hand, although the ternary inverters comprising the above devices demonstrated three distinct logic states, the instability of the ambipolar 2D materials and organics and the large V_{DD} values restrict the deployment of

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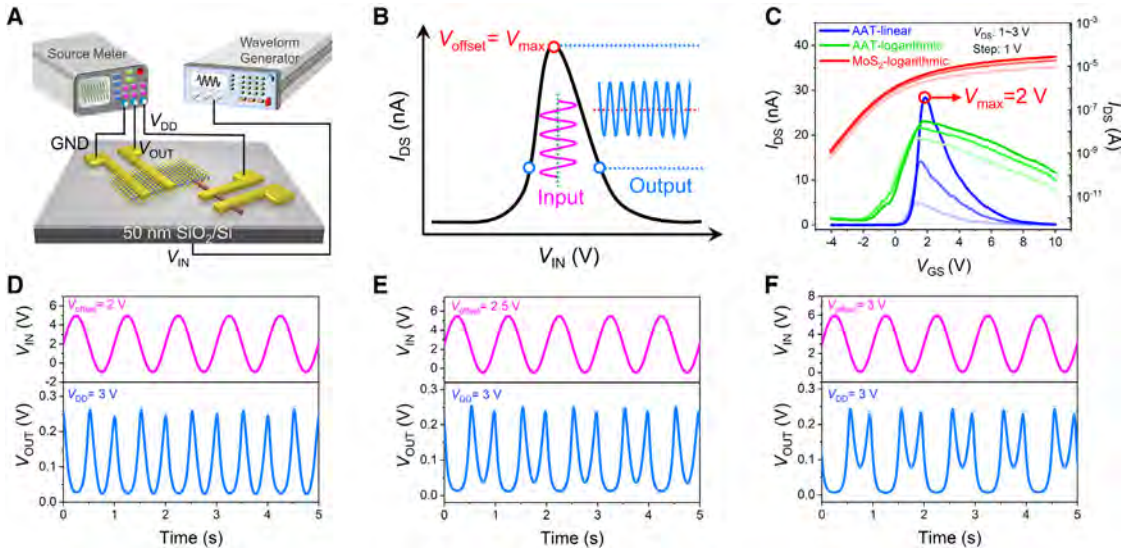

Figure 5. Frequency doubling circuit composed of GaAsSb/MoS_2 AAT device in series with MoS_2 FET

(A) Schematic illustration of the measurement configuration for frequency doubling based on the MoS_2 nanoflake FET and GaAsSb/MoS_2 AAT device.

(B) Schematic of the principle of frequency doubling based on anti-ambipolar transfer characteristics of GaAsSb/MoS_2 heterojunction device.

(C) Representative transfer characteristics of the GaAsSb/MoS_2 AAT device (linear in blue and semilog in green) and MoS_2 nanoflake FET (semilog in red) in the frequency doubling circuits.

(D–F) Input signal (pink) and output signal (blue) for the three different offset voltage values. Complete frequency doubling is observed when $V_{offset} = V_{max}$. More complicated signal conditioning occurs when V_{offset} is tuned away from V_{max}.

these MVL devices for practical applications. On the other hand, the transfer characteristics of the AAT device based on the ambipolar FETs make it difficult to realize the subsequent frequency doubling functionality.

Frequency doubling circuits

Apart from the application in logic circuits such as ternary inverters, the AAT device's anti-ambipolar characteristics also facilitate the realization of analog signal processing circuits, including frequency doubling functionality, which enables broad applications from analog communication to terahertz sensing.[32,52] Figure 5A shows the schematic illustration of the measurement configuration for frequency doubling based on the MoS_2 nanoflake FET and GaAsSb/MoS_2 AAT device. The V_{DD} was applied to the electrode on the NW side of the AAT, while the output signal (V_{OUT}) was measured from the voltage across the MoS_2 FET. The V_{DD} and V_{OUT} were provided and measured by the precision source/measure unit. The waveform generator was used to apply the sinusoidal input signal to the heterojunction device and MoS_2 FET through the 50-nm SiO_2/Si back gate. Since the resistance variation is obviously more considerable in AAT than in MoS_2 FET (Figure 5C), the MoS_2 FET can be considered equivalent to a roughly constant resistor. Figure 5B illustrates the working principle of the frequency doubling circuits based on the anti-ambipolar transfer curve. Generally, the frequency doubling is closely associated with positive and negative transconductances on the left and right sides of the current maximum. When an AAT is biased such that $V_{IN} < V_{max}$, the transconductance is positive with the current rising and the V_{OUT} across the MoS_2 FET increasing with the positive phase of the input signal. The case where $V_{IN} > V_{max}$ is analogous, but the V_{OUT} is out of phase with the V_{IN} because the input signal undergoes a negative transconductance with the increase of voltage. Besides, when $V_{IN} = V_{max}$, the transconductance turns to zero, leading to the local maxima of V_{OUT} whenever the input signal crosses V_{max} in either direction. As shown in Figure 5D, when the V_{offset} of the input signal is set equal to V_{max} of 2 V (derived from Figure 5C), the output signal oscillates at a double frequency compared to the input waveform, successfully demonstrating the practical application in frequency doubling for AAT devices. Another frequency multiplier with the same device configuration is exhibited in Figure S16. When V_{offset} deviates from V_{max}, the waveform of the frequency doubling gradually becomes incomplete (Figures 5E and 5F), which further supports the circuit operation model as stated. As a matter of course, the MoS_2 FET can also be substituted with a resistor of 1 MΩ (Figures S17A–S17C). Benefiting from the stable and unchanged resistance for the resistive load with voltage sweep, the frequency response of the GaAsSb/MoS_2 AAT-based device is then pushed to 100 Hz and 200 Hz, at which most of the output power is concentrated at the doubled fundamental frequency of 200 Hz and 400 Hz, respectively (Figures S17D and S17E). The refinements, such as applying encapsulation and local gating, will likely enable higher operating frequency due to air isolation and low parasitic capacitance.

DISCUSSION

An effective size downscaling approach was developed to realize tunable and high-performance AAT devices based on

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mixed-dimensional GaAsSb NW/MoS_2 nanoflake heterojunctions, which have significant advantages over the GaAsSb/MoS_2 in-series FETs in terms of wiring density and power consumption. The proper energy band alignment of the components allows the AAT device to be gate-tunable with an asymmetric anti-ambipolar transfer characteristic. Under the negative or positive extreme gate bias range, the device is doped as a p^+-i or i-n^+ junction, leading to low conductance of the AAT device with a high PVR of over 10^3 for both sides. With tailoring the channel size and carrier density, the anti-ambipolarity of AAT devices, including the peak position, on-state current level, and range, can be readily engineered in this device configuration, contributing to flexibly designing versatile electronics. Therefore, the synthetic performance of the designed AAT device was enhanced significantly by the configuration of the mixed-dimensional 1D GaAsSb NW/2D MoS_2 nanoflake heterostructure. The synergistic effect of high-mobility III-V NW and transition metal dichalcogenide (TMD) nanosheets ensures the high charge carrier transport efficiency in the AAT device channel. Besides, the active region downscaling can improve the frequency characteristics and energy efficiency of the AAT device in rectifying circuits, multivalued logic circuits, and frequency multipliers.

After integrating the AAT and unipolar transistor (GaAsSb p-FET/MoS_2 n-FET) into a unit device, the multifunctionality of the ternary logic inverter and frequency multiplier is realized synchronously for the first time. A typical ternary inverter can be implemented with three stable logic states by load matching. Also, the conspicuous intermediate logic state in the MVL device is free from the influence of applied drain bias. In contrast, it depends on the resistance ratio between the two components under gate bias. In comparison, although the reported heterojunctions, such as SWCNT/α-IGZO, pentacene/MoS_2, and carbon nanotube/MoS_2, exhibit typical anti-ambipolar behavior,[32,42,43] the MVL function could not be achieved without delicate design and modulation of the device structures.

Finally, the frequency doubling for the unique AAT device has been realized by exploiting the feature of sign-changing transconductance to validate its good capacity in analog signal processing. The traditional approach is to introduce a series-connected accessional constant resistor to obtain the frequency doubling function based on the AAT device,[32] which undoubtedly increases the complexity of the device architecture. By contrast, in our work, the frequency doubling circuits can be well implemented based on the GaAsSb/MoS_2 AAT device in series with an adjoining MoS_2 FET. This device configuration is beneficial to the flexible design and undemanding fabrication of frequency multipliers. Overall, the mixed-dimensional 1D GaAsSb NW/2D MoS_2 nanoflake heterostructure can effectively improve frequency characteristics and power consumption through the active region downscaling. More importantly, the series-connected unipolar p/n-FET with the AAT device could synchronously achieve the MVL and frequency doubling circuits by tuning the device parameters discreetly, which was demonstrated for the first time in the field of AAT applications. Therefore, the high performance and versatility of the mixed-dimensional AAT device promise great potential for the future development of more advanced and multifunctional integrated circuits.

EXPERIMENTAL PROCEDURES

Resource availability

Lead contact

Further information and requests for resources should be directed to and will be fulfilled by the lead contact, Johnny C. Ho (johnnyho@cityu.edu.hk).

Materials availability

This study did not generate new unique reagents.

Data and code availability

Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

Nanowire synthesis and characterization

The GaAsSb NWs were grown by a thiourea-assisted solid-source CVD method based on the vapor-liquid-solid mechanism. The dual-zone horizontal tube furnace includes upstream and downstream zones in the CVD system. Initially, a SiO_2/Si substrate (50-nm-thick thermally grown oxide) coated with 0.5-nm-thick Au catalyst film was placed in the center of the quartz tube of the downstream zone. Then, the thiourea and well-mixed GaSb/GaAs powders with a designated weight ratio (2:1 in wt %) were positioned in the middle of the two zones and the center of the quartz tube of the upstream zone, respectively, serving as surface passivation agent and solid source. After the pressure in the system was evacuated down to 2.0×10^{-3} torr, 100 sccm H_2 gas (99.999% purity) was introduced into the quartz tube. Next, both upstream and downstream zones were heated to 750°C and 610°C in 9 min, respectively. After holding at those temperatures for 12 min, the system was cooled naturally to room temperature in an H_2 atmosphere. The surface morphology of the as-grown NWs was examined by a field emission scanning electron microscope (SEM) (XL30, FEI/Philips). Crystal structures of the NWs were determined by high-resolution transmission electron microscope (TEM) imaging (2100F, JEOL). The elemental compositions were measured using an EDS detector attached to the TEM (CM-20, Philips).

Device fabrication and electrical measurements

The synthesized GaAsSb NWs were transferred on the SiO_2/Si substrate by drop-casting technique. Then the mechanically exfoliated MoS_2 nanoflake was stacked on top of the GaAsSb NW using a micro-manipulation transfer system to form the mixed-dimensional GaAsSb/MoS_2 heterojunction. Finally, Ni metal electrodes were patterned and deposited by direct laser writing lithography and electron-beam evaporation, respectively. The MoS_2 nanoflake transfer process can be found in Figure S18 and the supplemental experimental procedures in detail. The height profiles of the GaAsSb NWs and MoS_2 nanoflake were measured by AFM (Dimension Icon, Bruker). The Raman and μ-PL spectra were analyzed by a confocal microscope spectrometer (Alpha 300R, WITec). The electrical performance of fabricated AATs and ternary inverters was characterized by a standard electrical probe station and Agilent 4155C semiconductor analyzer. To assess the frequency doubling function, an arbitrary function generator (AFG-2005, GW Instek) and precision source/measure unit (B2912A, Keysight) were employed to provide the sinusoidal input signal and to collect the corresponding output signal.

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.device.2023.100184.

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AUTHOR CONTRIBUTIONS

J.C.H. and W.W. conceived the project. Y.M. performed the PL and Raman characterization. W.W., Y.M., and W.J.W. fabricated the devices and performed the electrical and optoelectronic experiments and data analysis, while P.S.X. and Q.Q. implemented the AFM, SEM, and TEM characterization and analysis. Z.X.L., B.W.L., D.J.L., D.C., and Y.Z.L. prepared the GaAsSb NW samples and carried out the basic material characterizations. J.C.H. and W.W. wrote the paper, assisted by S.P.Y., D.Y., and Y.X.Z. All authors examined and commented on the manuscript.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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