

Stability and Low-Frequency Noise in InAs NW Parallel-Array Thin-Film Transistors

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Abstract—In this letter, we present the dc characteristics, stability, and low-frequency noise (LFN) measurements, for n-type indium arsenide nanowire (NW) parallel-array thin-film transistors (TFTs) with a global back gate. These devices perform with mobilities ranging from 200–1200 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and produce a threshold voltage shift less than 0.25 V after 10 000 s of stress. The resulting LFN measurements indicate that the $1/f$ noise can be modeled by the number fluctuation model, at low drain currents, which can provide an essential guideline for the device design considerations of NW TFTs.

Index Terms—InAs, low-frequency noise, nanowire (NW) parallel arrays, stability, thin-film transistors (TFTs).

I. INTRODUCTION

DUE TO the high electron mobility and ease of near-ohmic metal contact formation, indium arsenide (InAs) nanowires (NWs) are promising alternative channel materials for high-performance transistors [1], [2]. Although there are several reports discussing the low-frequency noise (LFN) of FETs based on individual InAs NWs, by assessing FETs RF performance, there are limited studies on the electrical stability, dc characteristics, and $1/f$ characteristics of FETs based on InAs NW parallel arrays [3], [4]. All of these are important figures of merit for the practical implementation of NW thin-film transistors [5]. In general, a high degree of NW alignment, without NW crossing, is needed to achieve a high-performance NW thin film with low variation in gate electrostatics coupling and NW channel length. In this letter, we present, to the best of our knowledge, the first electrical stability and $1/f$ noise characterization of InAs NW parallel-array thin-film FETs. It is demonstrated that the $1/f$ noise seen

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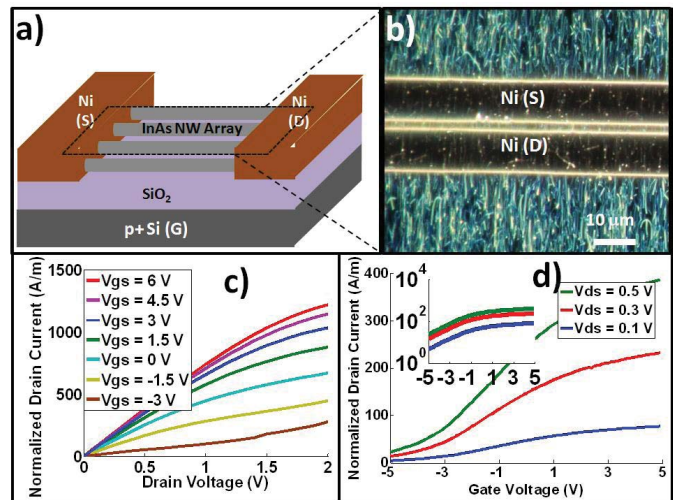


Fig. 1. (a) Schematic view of the InAs NW parallel-array TFT device. (b) Optical image of the NW parallel-array channel. (c) Output characteristics of the NW TFT (I_{ds} - V_{ds}). (d) Transfer characteristics of the NW TFT (I_{ds} - V_{gs} , with the log scale shown in the inset).

in the transistors can be primarily attributed to the change in the carrier concentrations, as described by the number fluctuation model.

II. FABRICATION AND EXPERIMENT

InAs NWs used in this study were synthesized using a catalytic chemical vapor deposition method similar to the ones previously reported [1], they were assembled by the contact printing technique [6] and passivated with a thin layer of ~ 25 -nm-thick electron-beam-evaporated silicon oxide (SiO_x). Fig. 1 shows a representative InAs NW parallel-array thin-film transistors (TFTs) fabricated with an effective channel width of 3 μm (physical channel width of 100 μm) and a channel length of 2 μm along with corresponding output and transfer characteristic curves. The effective width was calculated by multiplying the number of NWs (100) by the NW diameter (30 nm), commonly adopted in the nanowire community [1]. From the I_{ds} - V_{gs} plot, the threshold voltages were extracted to be -6.6 , -8.1 , and -9.4 V for TFT1, TFT2, and TFT3, respectively. The threshold voltages obtained are consistent with typical depletion-mode InAs NW FETs [1], [2]. The device mobilities and subthreshold slopes were extracted from these curves.

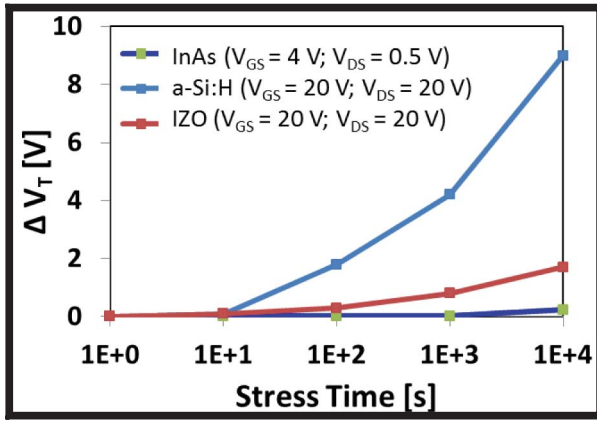


Fig. 2. Changes in V_T after 10000 s of dc stress for InAs, a-Si:H, and InZnO TFTs.

An investigation into the electrical stability of the NW arrays was conducted by stressing the TFTs for more than 100000 s with a gate bias of 4 V. Fig. 2 shows the voltage drift of each device with time by comparing the results with those for standard thin-film technologies such as a-Si:H and InZnO.

The LFN measurements were taken by measuring the current at the drain of NW parallel arrays with amplification using a FEMTO DLPCA-200 preamplifier for improved resolution. The signal was processed through a Hewlett Packard 4395A spectrum analyzer with a frequency range of 10 Hz to 100 kHz. All measurements were taken at room temperature and with a varied drain-source voltage ranging from 10 to 100 mV.

III. RESULTS AND DISCUSSION

The subthreshold slope, ranging from 2.72 to 4.14 V/dec, is mainly attributed to the back-gated device geometry as well as the large amount of surface traps existing in the NW oxide interface, which degrade the gate-coupling efficiency. Improvements in subthreshold slope could be realized in the future with better optimized device and dielectric structures [8]. Mobilities ranging from 200 to 1200 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ were recorded for these devices, with the large variation primarily due to the printing nonuniformity.

Fig. 2 shows that thin-film technologies such as a-Si:H and IZO display distinctly unstable dc characteristics after 10000 s electrical bias. The InAs NW TFTs remain relatively stable for prolonged periods of electrical stress with a threshold voltage shift less than 0.25 V. In contrast, a-Si:H and InZnO shift by almost 9 and 1.7 V, respectively [7]. Since the NW devices operate at significantly lower drive voltages than the compared devices, it inherently lowers the potential V_t shifts. Also, the single crystalline nature of InAs NWs is believed to contribute to this enhanced stability as well, which can be attributed to the low concentrations of defects such as dangling bonds, defect creation, and charge traps. These defects have varying degrees of impact on devices such as a-Si:H and IZO TFTs.

The current-normalized spectral densities (CNSDs) are shown in Fig. 3 and represent the LFN measurements recorded

from the drain of three NW parallel-array TFTs. The CNSD of a single NW, measured at 10 Hz, is around $7.3 \times 10^{-7} \text{ Hz}^{-1}$ [3], while the parallel array produced values ranging from 4.6×10^{-9} to $6.1 \times 10^{-6} \text{ Hz}^{-1}$, with a spread that was dispersed over roughly three orders of magnitude [3]. An even larger spread has been observed in Si NW transistors (four orders of magnitude) [9]. In the present InAs NW study, the observed spread is likely due to the large process variation typically experienced in a nonproduction research lab for processing the devices, and these variations are seen in all types of NW devices [3], [9]. Notably, the CNSD for each set of biasing conditions follows closely to the $1/f^\gamma$ dependency. In the McWhorter model [10] for LFN, the exponent γ indicates the uniformity of the relative gate oxide and interface traps with depth. When $\gamma = 1$, the trap densities are highly uniform in depth, while larger values indicate a larger trap density farther from the gate oxide interface and the reverse for smaller γ values [10], [11]. Fitting the log of the CNSD to a linear regression model produced frequency exponents valued at 1.02, 1.10, and 1.06, demonstrating the relatively uniform oxide trap distribution in our devices. For the data fitting, the frequency ranges that were dominated by 60 Hz noise were excluded from the data used for the linear regression fit, seen in Fig. 3(a). From the same fit, the oxide trap density can be calculated following the generalized drain current noise equation [10]:

$$\frac{S_{I_D}}{I_D^2} = \frac{q^2 k T \lambda N_t}{f^\gamma \text{WLC}_{\text{OX}}^2 (V_{\text{GS}} - V_T)^2}. \quad (1)$$

This generalized form based on the McWhorter model is grounded on the concept that carrier fluctuations are the primary source of $1/f$ noise in n-type transistors [10]. In (1), q is the charge of an electron, k is Boltzmann's constant, T is the temperature, N_t is the oxide trap density, and λ is the tunneling attenuation length, which is modeled as

$$\lambda = \left(\frac{4\pi}{h} \sqrt{2m^* \Phi_B} \right)^{-1} \quad (2)$$

using the Wentzel-Kramers-Brillouin theory, where h is Planck's constant, $m^* = 0.41m_0$ is the electron (hole) effective mass in the gate oxide, and $\Phi_B = 4 \text{ eV}$ is the tunneling barrier height the carriers see at the gate oxide interface [10].

The V_T was calculated to be -6.6 V , $L_g = 2 \text{ }\mu\text{m}$, $W_{\text{eff}} = 3 \text{ }\mu\text{m}$, and $C_{\text{OX}} = 0.056 \text{ fF}/\mu\text{m}^2$ for TFT 3. The best-fit approximation produced an oxide trap density of $\sim 9.88 \times 10^{17} \text{ cm}^{-3}\text{eV}^{-1}$. For TFT 1 and TFT 2, the trap densities were calculated to be 3.58×10^{21} and $5.93 \times 10^{21} \text{ cm}^{-3}\text{eV}^{-1}$, respectively. The estimated trap density values are larger than that of a typical polysilicon gate transistor, which has observable densities around $5 \times 10^{17} \text{ cm}^{-3}\text{eV}^{-1}$ [11], but are comparable to the values for some Si NW devices and multigate devices with ultrathin channels reported in [9] and [12].

Fig. 3(b) and (c) are log-log plots of CNSD noise versus current for two different TFT devices. The current is biased at $0.1 V_{\text{DS}}$ and is increased from -10 to $4 V_{\text{GS}}$ by increments of 1 V. The data are compared with $(g_m/I_{\text{ds}})^2$, to which noise is proportional to. This reveals, by inspection, that

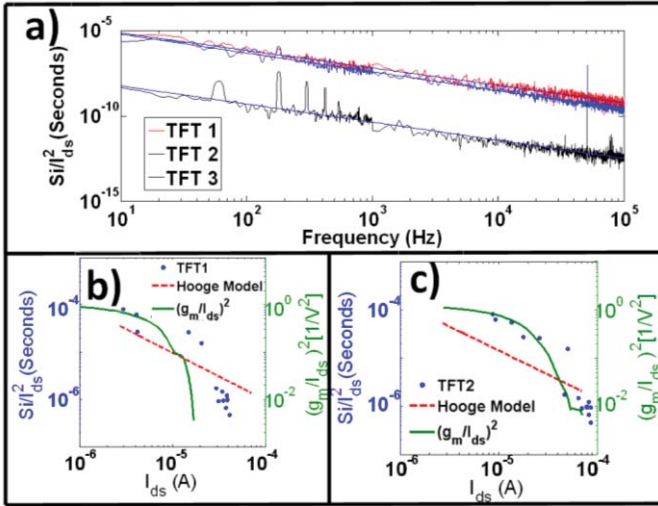


Fig. 3. (a) CNSD response from three NW parallel-array TFT devices biased at $V_{gs} = 0.5$ V and $V_{ds} = 0.1$ V. NW TFT 1 had an $L_g = 4$ μm , $W_{g,\text{eff}} = 3$ μm ($W_{g,\text{physical}} = 100$ μm), and $I_D = 21.95$ μA . NW TFT 2 had an $L_g = 6$ μm , $W_{g,\text{eff}} = 6$ μm ($W_{g,\text{physical}} = 200$ μm), and $I_D = 37.2$ μA . NW TFT 3 had an $L_g = 2$ μm , $W_{g,\text{eff}} = 3$ μm ($W_{g,\text{physical}} = 100$ μm), and $I_D = 184.0$ μA . (b) and (c) CNSD for two NW parallel-array devices versus current, compared with g_m^2/I_{ds}^2 .

the noise more closely follows the number fluctuation model given as [10]

$$S_{I_D} = S_{V_{\text{fb}}} \left(1 + \frac{\alpha \mu_{\text{eff}} C_{\text{OX}} I_D}{g_m} \right)^2 g_m^2 \quad (3)$$

$$S_{V_{\text{fb}}} = \frac{q^2 k T \lambda N_t}{f^2 W L C_{\text{OX}}^2} \quad (4)$$

where α is the scattering parameter of the mobility fluctuations and their correlation to the number fluctuations, and the variables correspond to those of (1). Eqs. (3) and (4) describe the data in Fig. 3(b) and (c) more completely than (1), indicating that the noise behavior is reasonably well described by the number fluctuation model. This is the same noise model which the single NW devices were also found to follow [3].

The competing model in use is known as the Hooge model which attributes the $1/f$ noise properties to mobility fluctuations. The model can be written as (5) which reveals that the $1/f$ noise should be proportional to the inverse of the drain current

$$\frac{S_{I_D}}{I_D^2} = \frac{\alpha_H \mu_{\text{eff}} 2kT}{f L^2 I_D} \quad (5)$$

where α_H is the Hooge's parameter, μ_{eff} is the effective mobility, and the rest of the variables are the same as in (1). Theoretical curves based on (5) are compared to the measured data in Fig. 3, and it becomes clear that the Hooge's model fails to represent the data accurately over a large range of biasing. The Hooge parameter can be extracted using the normalized current spectral densities in Fig. 3(b) and (c). Hooge parameters for vertical single NW InAs transistors and lateral single NW InAs transistors have been reported to be

4.2×10^{-3} [3] and 8.4×10^{-3} [4], respectively. Values extracted from some of the tested devices were seen to reach $\sim 10^{-3}$, this was only for a small range of biasing. In general, the calculated Hooge values were roughly three to five orders of magnitudes larger, further supporting the idea that the McWhorter model, in general, provides a better description [10]. Therefore, since the data are best fit with the number fluctuation model, we can attribute the LFN to fluctuations in the carrier concentration caused by trapping and detrapping at and inside the gate oxide.

IV. CONCLUSION

In this letter, the dc characteristics and device stabilities were reported for parallel-arrayed InAs NW transistors. These transistors were found to perform with mobilities up to two to three orders of magnitude larger than the current technologies, such as a-Si:H, and with 10 times the stability. The $1/f$ noise was also investigated and produced spectral densities which were comparable to that of other similar single NW devices and had relatively uniform trap densities in the oxide.

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