Stable Hysteresis-Free MoS_2 Transistors With Low-k/High-k Bilayer Gate Dielectrics

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***Abstract*— Hysteresis-free and low-voltage operation are essential for low-power-consumption electronics. Herein, MoS_2 transistors configured with bilayer-stacked polymethyl methacrylate (PMMA)/poly (vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) gate dielectric are demonstrated, which leverages the advantages of the hysteresis-free characteristic of PMMA and high-*k* property of P(VDF-TrFE). The trap density and the threshold voltage of the devices can be reduced to 7.0×10^{11} $cm^{-2} \cdot eV^{-1}$ and −2.2 V, respectively. Moreover, the devices maintain stable performance under bias stress conditions. The devices present negligibly changed transfer and output characteristics over 101 cycling tests, indicating excellent stability. The bilayered dielectric engineering strategy provides a promising avenue to achieve hysteresis-free low-power operation in 2D materials based transistors with high stability.**

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***Index Terms*— Bilayer dielectrics, MoS_2, hysteresis-free, high stability.**

I. Introduction

As the device miniaturization is approaching its fundamental physical limit, alternative device channel materials [1], such as two-dimensional (2D) layered materials with atomic thickness, present excellent electrical performance even with 1 nm short channel [2]. Generally, the threshold voltage (V_{TH}) is predominantly dictated by the thickness and the relative permittivity of gate dielectrics. Ultrathin high-*k* oxide dielectrics, *e.g.* HfO_2 [3], are utilized for low-voltage operation, where the enhanced electrostatic gate control can be efficiently achieved. However, the conformal deposition of dielectrics on MoS_2 still remains challenging, due to the lack of sufficient dangling bond or nucleation sites [4]. On the other hand, solution-processed high-*k* polymer dielectrics, such as poly (vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)), are widely considered as high-quality dielectric layers for 2D materials based transistors [5]–[7].

Nevertheless, there is still a disastrous disadvantage that the localized states induced by the gate bias would lead to significant numerous trapped charges existed in the 2D materials/dielectric interface, which makes the V_{TH} shift substantially even in the inert environment [8]. To address this stability concern, low-*k* non-polar polymer dielectrics have been adopted [9]. And a low-*k* hydrophobic dielectric, such as polymethyl methacrylate (PMMA), enables hysteresis-free operation by eliminating the influence of moisture, oxygen, mobile charges, and some other impurities [10], but the fabricated devices cannot be operated with low voltage.

In this regard, the bilayer-stacked dielectrics are proposed, in which the high-*k* dielectrics induce high accumulated carrier density in the channel with high gate capacitance, whereas the low-*k* dielectrics provide the device with the reasonably stable operation. Herein, the bilayer-stacked dielectrics, which consist of low-*k* PMMA and high-*k* P(VDF-TrFE), are employed to achieve high-performance MoS_2 transistors with the low-voltage operation, hysteresis-free characteristic, and long-term stability. Notably, the interface trap density (D_{it}) and V_{TH} can be reduced to be 7.0×10^{11} $cm^{-2} \cdot eV^{-1}$ and −2.2 V, respectively. Therefore, the strategy present here is

the potential for fabricating low-power and hysteresis-free 2D materials based transistors with excellent stability.

II. Experimental

The structure of bilayered-stacked dielectrics was shown in Fig. 1a. The source/drain region is defined by e-beam lithography (EBL). And the Cr/Au (15 nm/45 nm) electrodes were deposited by the thermal evaporator and lift-off processes. Subsequently, the PMMA solution (20 *wt.*%) in methyl ketone was spin-coated onto the substrate at the speed of 3500 rpm for 1 min, followed by annealing on a hot plate at 150 °C for 2 min. The thickness of PMMA is about 45 nm that confirmed by the ellipsometer (α-SETM, J.A. Woollam. Co., Inc). The thin P(VDF-TrFE) layer was later formed by the spin-coating method at 4000 rpm for 1 min and then was baked at 130 °C for 30 min. The total thickness of PMMA/P(VDF-TrFE) dielectric layer was about 95 nm. To avoid the electron irradiation in the EBL process, a 40 nm Au top-gate electrode, the radius of which is about 25μm, was deposited with a shadow mask as shown in the inset of Fig. 1b. The fabricated device was shown in Fig. 1b, and the channel length of the device is 3 μm. For the devices with individual PMMA and P(VDF-TrFE) dielectric, the spin-coating speed was set to 3000 r/min, and the thicknesses of PMMA and P(VDF-TrFE) dielectric layer were controlled to be about 95 nm. At last, electrical characteristics of all devices were performed using a Lake Shore TTPX probe station and an Agilent B1500A semiconductor parameter analyzer in the vacuum conditions.

III. Results and Discussion

The P-E properties of PMMA, P(VDF-TrFE), and PMMA/P(VDF-TrFE) were tested on the superconducting quantum interface device magnetometer (Quantum Design PPMS-9), as shown in Fig. 1c. The P(VDF-TrFE) dielectric layer yields a typical ferroelectric polarization phenomenon with a corrective voltage of ~14.9 V and a residual polarization value of ~7.4 μC · cm^{-2}. As a nonpolar polymer, the polarization *versus* voltage (*P*-*V*) curve of PMMA indicates hysteresis-free characteristics. On the other hand, due to the electrostatic screening effect of the PMMA layer and the low partial voltage, the PMMA/P(VDF-TrFE) dielectrics show negligible ferroelectric characteristics.

Fig. 1d-f display typical transfer curves of the fabricated MoS_2 transistors integrated with different gate dielectrics. Since monolayer MoS_2 transistors typically exhibit low carrier mobility and high contact resistance, few-layer MoS_2 flakes with a thickness of around 4.5 nm are utilized as the channel layer. Due to the non-linear property of the ferroelectric P(VDF-TrFE), anti-clockwise transfer curves of the devices integrated with P(VDF-TrFE) dielectric layer present a voltage hysteresis (ΔV_{TH}) of ~0.7 V (Fig. 1d). The hysteresis is often originated from the ferroelectric of P(VDF-TrFE) [11]. Since PMMA is a nonpolar hydrophobic polymer that can be crystallized at low temperatures, the aforementioned influence of moisture, oxygen, mobile charges, and other impurities can be suppressed [12]. Therefore, the device with PMMA dielectric exhibits a small ΔV_{TH} of 0.3 V, as shown in Fig.1e and

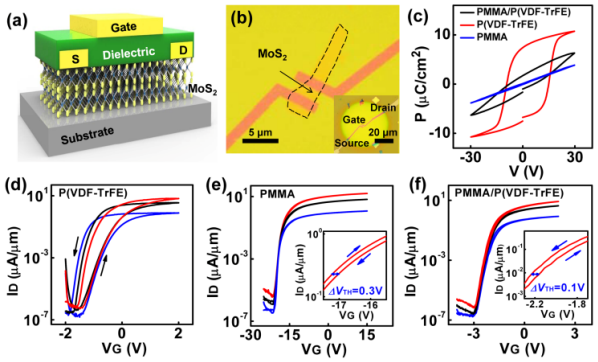

Fig. 1. (a) Schematic image of the top-gated MoS_2 transistors with different gate dielectric layers: P(VDF-TrFE), PMMA, and PMMA/P(VDF-TrFE). (b) The optical micrograph shows the contact between MoS_2 and metal electrodes, and the inset is the global image of the MoS_2 transistor. (c) Ferroelectric polarization characteristics of the dielectrics. (d)-(f) Typical transfer curves of the MoS_2 transistors with different gate dielectrics. The red line, black line, and blue line is corresponding to V_D = 1 V, 0.5 V, and 0.1 V, receptively. The insets are the zoom in the curves of the transfer characteristic with V_D = 1 V.

the inset. The PMMA/P(VDF-TrFE) bilayer-stacked dielectric can leverage the hysteresis-free operation of PMMA as well as the high-*k* property of P(VDF-TrFE), rendering small ΔV_{TH} of 0.1 V with a low V_{TH} of −2.2 V (Fig. 1f and inset).

To further evaluate the interface quality of the devices, the corresponding D_{it} is assessed, which can be extracted by the equation:

$$D_{it} = \frac{c_i}{q}\left(\frac{q \cdot SS}{kT \ln 10} - 1\right) \tag{1}$$

where C_i is the capacitance per unit area, q is the electric charge, k is the Boltzmann constant, T is the temperature, and SS is subthreshold swing [13]. As the C_i is measured to be 70.0 nF · cm^{-2} for PMMA/P(VDF-TrFE) dielectric with a semiconductor parametric analyzer (Keithley 4200-SCS), and the dielectric constant of P(VDF-TrFE) and PMMA are 8.0 and 3.3, respectively [10], [14]. In this way, the D_{it} values of the P(VDF-TrFE), PMMA and bilayer stack are determined to be 7.4×10^{11} cm^{-2} · eV^{-1}, 9.0×10^{11} cm^{-2} · eV^{-1}, and 7.0×10^{11} cm^{-2} · eV^{-1}, respectively. The results indicate that PMMA could form a high-quality interface with MoS_2 with low interface trap density.

As shown in Fig. 2a, the device with P(VDF-TrFE) dielectric shows a decreased on-state current with negative bias stress (NBS) time, which could be explained by the polarization and fatigue of P(VDF-TrFE) dielectric [15]. Under the negative electric field, the polarization direction of P(VDF-TrFE) directs from channel to gate, thereby pulling up the conduction band level and depleting electron in the channel. Additionally, the transfer curves of the devices with P(VDF-TrFE) dielectric shifts towards the negative direction because of the fatigue of ferroelectrics under electrical stress. The fatigue of ferroelectrics reveals decreased remnant polarization and increased coercive field, resulting in applying a larger gate voltage, which further leads to the on-state current variation under bias stress condition [16], [17]. Because of the excellent stability of PMMA, stable channel current and ΔV_{TH} for devices are obtained in the vacuum conditions (Fig. 2b). The devices with PMMA/P(VDF-TrFE) bilayer dielectrics

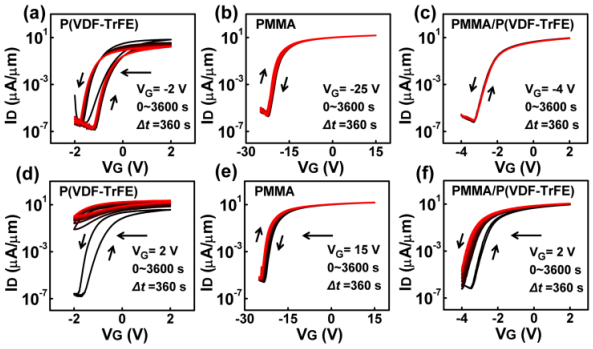

Fig. 2. I_D-V_G curves of the MoS_2 transistors with P(VDF-TrFE), PMMA, PMMA/P(VDF-TrFE) bilayer dielectrics, under (a-c) NBS at $V_D = 1$ V and (d-f) PBS at $V_D = 1$ V.

present the consistent transfer characteristics under NBS condition (Fig. 2c).

As shown in Fig. 2d, the on-state current of the MoS_2 transistors with P(VDF-TrFE) dielectric show the on-state current increases from 3.6 μA/μm to 23.5 μA/μm with positive bias stress (PBS) time and a negative shift of V_{TH} after 3600 s, owing to the fatigue of ferroelectric under bias stress. Under PBS conditions, the polarization of P(VDF-TrFE) induces accumulated electron in the channel, so that the electron concentration is increased after PBS. The on-state current almost maintains consistent values for both of the devices with PMMA and PMMA/P(VDF-TrFE) as dielectric (Fig 2e and f). The V_{TH} of MoS_2 transistors with PMMA/P(VDF-TrFE) dielectrics is around -0.75 V after 3600 s under PBS condition, indicating superior stability of the devices with PMMA/P(VDF-TrFE) bilayer dielectrics. As Illarionov et al demonstrated, the V_{TH} shift in MoS_2 transistors can be explained by the assuming charging/discharging of the defects [18].

The results of the bias stress test indicate the stability of MoS_2 transistor with bilayer dielectrics originates from the PMMA layer, and the PMMA prevents the interdiffusion actions at the ferroelectric P(VDF-TrFE) interfaces, leading to the robust reliability and stability of the MoS_2 transistors [19].

Fig. 3a presents the 101 measurement cycles with a test procedure lasting for 5 h, which is performed in vacuum condition, and the gate voltage sweeps from negative to positive and then back to a negative value in each cycle. Combined with the unchanged hysteresis loop, the results indicate excellent reliability of the MoS_2 transistors with PMMA/P(VDF-TrFE) bilayer dielectrics. Fig. 3b plots the corresponding output curves of the 1st cycle and the 101st cycle, showing unchanged output characteristics. Fig. 3c exhibits the ΔV_{TH} and current variation ratio ($\Delta I/I_0$) as a function of gate voltage sweeping cycles, which indicates the negligible variation of the device performance.

Low-frequency noise characterization is utilized to quantitatively analyze the performance and reliability of MoS_2 transistors. The noise spectra can be obtained by the equation:

$$S_{ID} = I_D^{\beta} \Big/ f^{\gamma} \tag{2}$$

where β and γ are the exponents on-state current and frequency (f), respectively [20]. The Agilent B1500A and

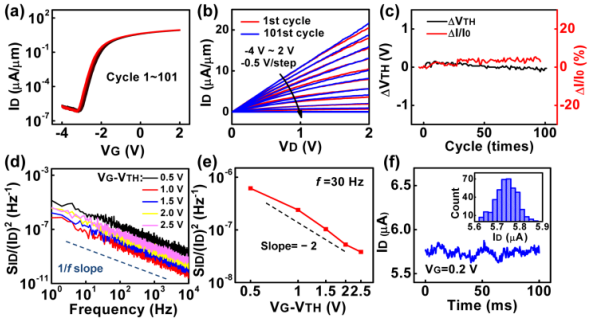

Fig. 3. (a) Transfer curves of the MoS_2 transistors with PMMA/P(VDF-TrFE) bilayer dielectrics during 101-cycles measurements. (b) Typical output curves of the 1st cycle and the 101st cycle. (c) ΔV_{TH} and $\Delta I/I_0$ during cycle measurements. (d) Noise spectra of the MoS_2 transistor gated by PMMA/P(VDF-TrFE) with $V_D = 0.5$ V. (e) Noise spectra dependence of the effective gate voltage at 30 Hz. (f) I_D fluctuation of the MoS_2 transistors with PMMA/P(VDF-TrFE) bilayer dielectrics.

E5052B with a resistor unit were used to analyze the low-frequency $1/f$ noise of devices.

As shown in Fig. 3d, the power spectral density of channel current fluctuation (S_{ID}) is calculated based on the channel current as a function of time. Linear fitting is carried out for the logarithmic ratio of S_{ID}/I_D^2 and $1/f$. An ideal γ value of -1 is obtained. Therefore, the $1/f$ noise characteristic is inferred, suggesting the noise is originated from the carrier number fluctuation. Fig. 3e is the plots of extracted S_{ID}/I_D^2 under different gate voltages when $f = 30$ Hz. The plot of power spectral density *versus* gate voltage shows a linear relationship in logarithmic coordinates with a slop approaching -2 (Fig. 3e). This variation conforms to the description of McWhorter model, in which the $1/f$ noise is mainly caused by the carrier number fluctuation in the top-gated transistors with bilayer dielectrics [21]. In the theory of fluctuation mechanism of carrier number, trap defects in the dielectric interface randomly capture and release electrons, leading to the fluctuation of carrier concentration in the channel, thus generating the noise phenomenon [22]. The channel current fluctuation is an alternative method to quantitatively analyze performance, variability, and reliability of highly scaled devices. Fig. 3f presents the channel current at different times during low-frequency noise measurement, and the sampling rate is 0.25 ms/point. The inset in Fig. 3f is the statistical distribution of current extracted from Fig 3f. The channel current negligibly changes with time, exhibiting the bias stress stability and low traps density in the devices.

IV. Conclusion

Low-voltage hysteresis-free MoS_2 transistors with excellent stability are fabricated by employing a low-k/high-k configuration of PMMA/P(VDF-TrFE) bilayer dielectrics. The high-k dielectric affords high accumulated carrier density, while the low-k dielectric promises the reasonably stable operation. The devices can not only retain low-voltage operation but also realize long-term stability. This work provides an alternative approach to fabricate high-performance 2D materials transistors with low-power consumption and hysteresis-free operation.

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