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Surface roughness induced electron mobility degradation in InAs nanowires

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Abstract
In this work, we present a study of the surface roughness dependent electron mobility in InAs nanowires grown by the nickel-catalyzed chemical vapor deposition method. These nanowires have good crystallinity, well-controlled surface morphology without any surface coating or tapering and an excellent peak field-effect mobility up to 15 000 $cm^2 V^{-1} s^{-1}$ when configured into back-gated field-effect nanowire transistors. Detailed electrical characterizations reveal that the electron mobility degrades monotonically with increasing surface roughness and diameter scaling, while low-temperature measurements further decouple the effects of surface/interface traps and phonon scattering, highlighting the dominant impact of surface roughness scattering on the electron mobility for miniaturized and surface disordered nanowires. All these factors suggest that careful consideration of nanowire geometries and surface condition is required for designing devices with optimal performance.

S Online supplementary data available from stacks.iop.org/Nano/24/375202/mmedia

(Some figures may appear in colour only in the online journal)

1. Introduction

Recently, III–V semiconductor nanowires (NWs) such as InAs have been extensively studied as channel materials for high-performance transistors because of their high electron mobility and their ability to readily form near-Ohmic metal contacts [1–8]. At the same time, due to their one-dimensional geometric nature with an extraordinarily high surface-to-volume ratio, the electrical transport properties of these NWs are observed to be heavily dependent on their dimension and surface condition [3, 5, 9–16]. In particular, when the NW diameter is aggressively scaled for better electrostatics and lower leakage current, the field-effect mobility is found to decrease accordingly [17, 18], suggesting the impact of enhanced surface roughness scattering for electrons in miniaturized NWs [3, 9, 14, 15]. Theoretically, the surface roughness is shown to induce significant changes in the NW electronic band structure and to modulate its transport properties, including carrier mean free paths, mobilities and others [19–21]. However, as of today, there are few experimental reports directly assessing the effect of surface roughness on the electron mobility of NWs. In this work, we present a semi-quantitative study of the surface roughness dependent electron field-effect mobility of InAs NWs, in which the intrinsic electron mobility is demonstrated to decrease monotonically with increasing NW surface roughness. Low-temperature electrical device characterization further elucidates the dominant role

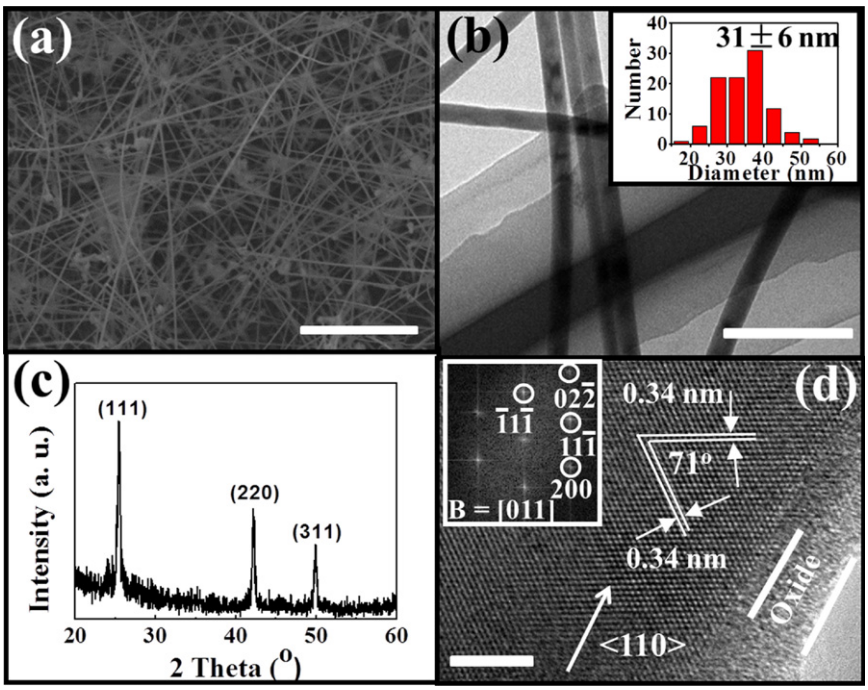

Figure 1. (a) SEM image of the as-obtained InAs NWs (scale bar = 2 μm). (b) TEM image of the NWs depicted in panel (a) (scale bar = 200 nm). The inset shows the diameter statistics of 100 NWs observed in the TEM study. (c) XRD spectrum of the grown NWs. (d) High-resolution TEM image of a representative NW shown in panel (a) (scale bar = 5 nm). The inset displays the corresponding fast Fourier transform reciprocal lattice spots where the [110] zone axis is identified.

of surface roughness scattering in the degradation of electron mobility in scaled and surface disordered NWs. All this information is critical for designing NW geometries to achieve optimal and practical device performances.

2. Experimental details

The InAs NWs used in this study were prepared by a solid-source catalytic chemical vapor deposition (CVD) method as previously reported [1–4]. In brief, InAs powders (∼1.2 g; 99.9999% purity) were heated in the upstream zone (690 °C) of a two-zone tube furnace and the evaporated precursors were transported by a carrier gas H_2 (200 sccm) to the downstream zone (470 °C). In this zone, InAs NWs were grown utilizing the Ni catalyst film (0.2 nm thick and pre-annealed at 800 °C for 10 min) pre-deposited on SiO_2/Si substrates for 60 min. The pressure was maintained at ∼1.0 Torr. After cooling in the H_2 gas atmosphere, the grown NWs were harvested in anhydrous ethanol by sonication, then dropped onto a copper grid for transmission electron microscopy (TEM; JEOL 2100F) analysis and onto SiO_2/Si substrates (50 nm thermal grown oxide on degenerately doped Si) for fabrication of the back-gated field-effect transistor (FET). In this study, NW FETs were fabricated by the definition of electrodes using a standard lithography process, followed by the deposition of Ni (50 nm in thickness) and metal lift-off. It is noted that a 5 s HF (1%) etch was immediately applied prior to the Ni deposition in order to remove the NW native oxide to ensure the formation of Ohmic contact between the metal electrode and NW. The electrical properties of the fabricated devices were then characterized with a cryogenic probe station (Janis ST-500) and semiconductor parameter analyzer (Agilent 4155C).

3. Results and discussion

3.1. Crystalline InAs nanowires

As shown in figures 1(a) and (b), all as-grown NWs are straight, long and dense with a uniform diameter along their entire length; these conditions are essential in evaluating the intrinsic NW electrical transport properties in this work since any surface coating or tapering would significantly degrade the electrical properties of the NWs [22–24]. Also, based on the statistics of 100 individual NWs observed in TEM, the obtained NWs have an average diameter of 31 ± 6 nm, providing a wide distribution of NW geometries as well as surface roughness from the same growth run for device fabrication, to ensure a consistent comparison in this study. These wide distributions of NW diameter and surface roughness are believed to originate from the variation in dimension of the starting catalyst as well as the CVD growth process. Figures 1(c) and (d) further illustrate the crystallinity of the as-obtained NWs, which exhibit a zinc blende crystal structure with a dominant growth direction of ⟨110⟩ (supporting information figure S1 available at stacks.iop.org/Nano/24/375202/mmedia), agreeing with other InAs NWs reported in the literature [3, 25]. It has also been reported that thin InAs NWs grown by metalorganic vapour phase epitaxy and molecular beam epitaxy typically consist of the

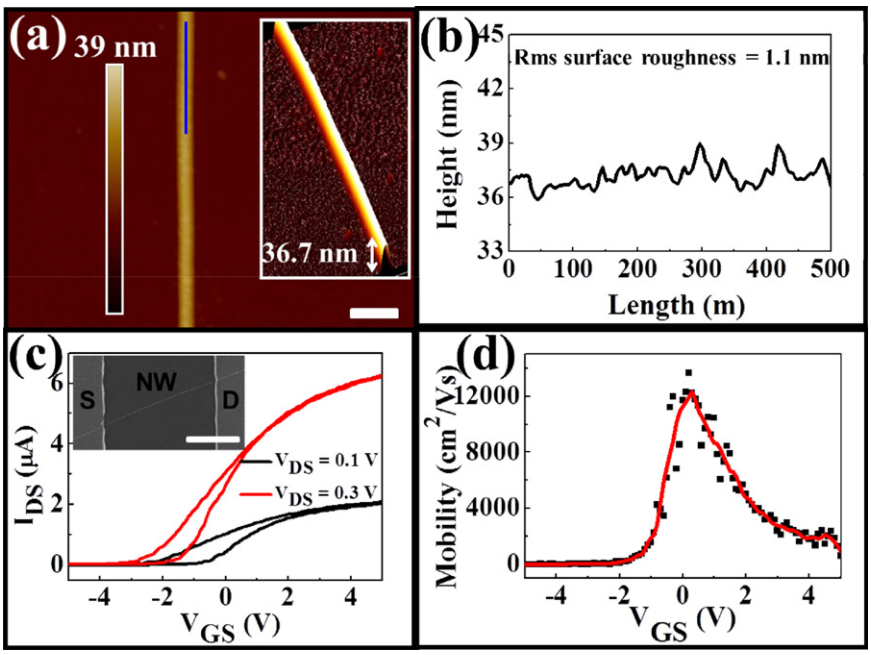

Figure 2. (a) 2D topographic AFM image of a representative NW (diameter $d = 36.7$ nm; surface roughness $= 1.1$ nm; scale bar $= 200$ nm). The inset shows the corresponding 3D image with the determination of NW diameter. (b) Height profile of the same NW by tracing along the line segment marked in blue in panel (a), demonstrating the magnitude of surface roughness in this particular NW. (c) Transfer characteristics of a back-gated InAs NW FET based on the NW illustrated in panel (a) (channel length ~ 10.0 μm; $V_{DS} = 0.1$ and 0.3 V). The inset depicts the corresponding SEM image of this NW device (scale bar $= 5$ μm). (d) Field-effect mobility assessment of the same device in panel (c) under $V_{DS} = 0.1$ V. The black dotted line gives the experiment data while the red solid line provides the fitted smooth data curve. A 3.0 nm thick native oxide shell is subtracted from the measured NW radius for the mobility calculation. It is also noted that all measurements presented here are taken at room temperature (298 K).

hexagonal wurtzite structure which is not observed here in our NWs [26, 27]. Notably, there is a thin layer of native oxide ($\sim$3 nm) on the NW surface; based on the detailed TEM investigation (figure 1(d)), the oxide layer is very conformal such that surface roughness measured in this work can truly represent the NW surface condition instead of the oxide roughness (supporting information figures S2 and S3 available at stacks.iop.org/Nano/24/375202/mmedia). Importantly, this oxide thickness will later be subtracted from the measured NW diameters to give the effective channel width for the subsequent mobility assessment.

3.2. Nanowire dimensions and surface roughness

In order to characterize the NW dimensions and surface roughness precisely, we first performed an atomic force microscopy (AFM) study of our NWs, already drop-casted onto the SiO_2/Si substrates. Two-dimensional (2D) and three-dimensional (3D) AFM topographic images of one representative NW are depicted in figure 2(a) and the inset which indicate that the NW indeed has a uniform diameter in the axial direction, and the corresponding diameter can be measured as 36.7 nm from the height determination of the 3D topograph. More importantly, the NW surface profile can then be obtained by tracing along the height or thickness of the NW; the root-mean-square (rms) surface roughness is found to be 1.1 nm, illustrating the relatively smooth surface of this particular NW (figure 2(b)) [9]. At the same time, room temperature electrical transport properties of the same NW can also be evaluated by configuring it into a back-gated NW FET as shown in figure 2(c). A long channel length of $\sim$10 μm is adopted here to ensure the diffusive transport of electrons (rather than ballistic or quasi-ballistic transport), from which intrinsic transport properties such as electron mobility can be deduced [3, 9]. In any case, the transfer characteristics (I_{DS}–V_{GS} curve) exhibit the n-type conductivity of InAs NWs as expected and a high ON current of $\sim$2 μA at $V_{DS} = 0.1$ V and $V_{GS} = 5$ V with a minimized electrical hysteresis observed in this ambient measuring environment, comparable to state-of-the-art InAs NW devices [3, 4, 17, 18]. The corresponding field-effect electron mobility (μ) is then calculated with the standard square-law model, $\mu = g_m(L^2/C_{ox})(1/V_{DS})$, where transconductance $g_m = (dI_{DS})/(dV_{GS})$ at a constant V_{DS} and C_{ox} is the gate capacitance modeled from the finite element analysis software COMSOL [28]. Notably, this capacitance value can also be calculated from the analytical expression $C_{ox} = 2\pi\varepsilon\varepsilon_o L/\cosh^{-1}[(r + t_{ox})/r]$, where ε is the dielectric constant of the gate insulator (3.9 for SiO_2), ε_0 is the permittivity of free space, L is the nanowire channel length, r is the nanowire radius and t_{ox} is the thickness of the gate oxide dielectric [3]. However, this calculated value is always roughly two times higher than the actual measured as well as the simulated values (e.g. $C_{ox} = 1.44$ fF from calculation versus $C_{ox} = 0.59$ fF from COMSOL for the device studied in figure 2), which typically underestimates the corresponding NW device mobility [3, 28]. Therefore,

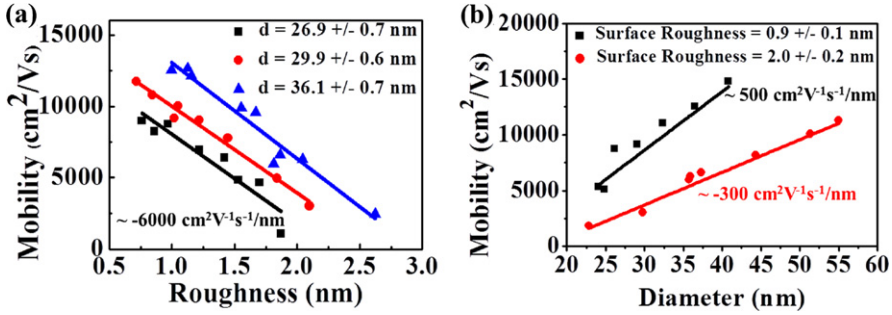

Figure 3. (a) Peak field-effect mobility as a function of surface roughness for NWs with three different diameter ranges: 26.9 ± 0.7 nm, 29.9 ± 0.6 and 36.1 ± 0.7 nm. Over this NW roughness range, the mobility decreases linearly with roughness, closely fitting the linear expression with a slope of around -6000 cm^2 V^{-1} s^{-1} nm^{-1}. (b) Peak field-effect mobility as a function of diameter for two different surface roughness ranges: 0.9 ± 0.1 and 2.0 ± 0.2 nm. Over this NW diameter range, the mobility increase linearly with diameter, closely fitting the linear expression with a slope of around 300 and 500 cm^2 V^{-1} s^{-1} nm^{-1} for NWs with roughness of 2.0 and 0.9 nm, respectively.

we adopt the simulated capacitance values for the mobility assessment in this work. As presented in figure 2(d), a respectable mobility of ∼12 000 cm^2 V^{-1} s^{-1} is attained for this particular NW device, in which this high mobility value can be attributed to the good crystallinity (figure 1), relatively large effective channel width and insignificant surface roughness.

3.3. Impact on field-effect mobility

To help investigate the effect of NW surface roughness on electron mobility, NW devices with a wide range of NW diameters and surface roughnesses are systematically selected and characterized at room temperature. Figure 3(a) gives the peak field-effect mobility as a function of rms surface roughness for NWs with three different diameter ranges: 26.9 ± 0.7 nm (thin), 29.9 ± 0.6 (medium) and 36.1 ± 0.7 nm (thick). It is not surprising that the thick NWs yield the highest mobility of all devices because of the larger effective channel width as well as the effect of a lower phonon scattering rate and surface scattering [3, 9, 17, 18]. Interestingly, the mobility is found to decrease monotonically with increasing roughness for all NW diameters here (∼27–37 nm) with a similar slope of around -6000 cm^2 V^{-1} s^{-1} nm^{-1}, indicating a consistent effect of surface roughness on mobility in this diameter range. This mobility degradation agrees well with the theory that surface roughness can easily induce changes in the local electronic band structures, which act like scattering potentials that scatter carriers moving in the NW, reducing the mean free time and mobility consequently [19–21]. For example, Ramayya *et al* used the ensemble Monte Carlo simulation method to demonstrate that an increase in the NW surface roughness would reduce the carrier mobility of Si NWs, which is in agreement with our experimental results [29]. The simulation also illustrates that increased NW dimension can enhance the carrier mobility, as revealed in figure 3(b) [29].

Moreover, as predicted, NWs with a rough surface (rms = 2.0 ± 0.2 nm) have a lower mobility than the smooth ones (rms = 0.9 ± 0.1 nm) in figure 3(b), and more importantly their mobility values are also less sensitive to the change in diameter (∼300 cm^2 V^{-1} s^{-1} nm^{-1}). This smaller sensitivity in the rough NWs is believed to be due to a stronger effective scattering potential, and the strength of this effective scattering potential mainly depends on the NW diameter d as well as the surface roughness [29]. When d increases, the roughness scattering potential is reduced as the electron can move in a larger NW cross-section and experience a smaller roughness effect with the mobility enhanced. For the greater roughness, the scattering effect is more significant since the roughness effect can penetrate deeper into the NW. In other words, when the roughness occupies a larger fraction of the NW cross-section, the modulation in the scattering potential induced by the change in NW diameter is less effective; therefore, the increase in mobility due to the increase in diameter is smaller in a rough NW. In this regard, when the surface roughness is higher, the slope is expected to be lower in figure 3(b); however, one could expect that this surface scattering effect would diminish for larger NW diameters (e.g. >100 nm or higher) since bulk transport scattering mechanisms such as acoustic phonon scattering dominate there [30].

Next, low-temperature electrical measurements were performed in order to further elucidate the role of surface roughness among all possible scattering mechanisms by decoupling the influence of phonon scattering and thermal activated surface/interface traps. As shown in figure 4(a), all mobility values with different surface roughness are improved at 77 K as all phonon modes and surface traps are fully frozen; however, this improvement is profound for smooth NWs but is less effective for rough NWs, highlighting the dominant effect of surface roughness induced scattering for surface disordered NWs. Moreover, the dependence of mobility on the NW dimension with surface roughness (rms = 2.0 ± 0.2 nm) was also investigated at both 298 and 77 K (figure 4(b)). Specifically, at 77 K where the phonon and traps were known to play a minor part in the reduction of mobility, there is only a small improvement in mobility for small NW diameters, illustrating the significance of surface scattering in the miniaturized NWs since smaller NWs have a larger surface-area-to-volume ratio and thus their surface properties are more dominant. All these results experimentally demonstrate and quantify the impact of enhanced surface

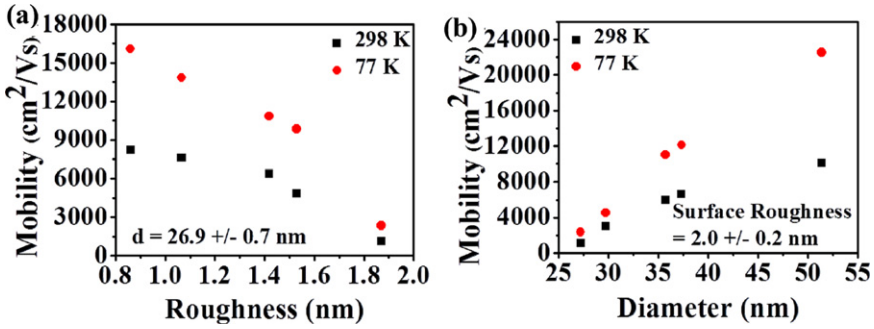

Figure 4. The dependency of peak field-effect mobility on (a) NW surface roughness (diameter $= 26.9 \pm 0.7$ nm) and (b) NW diameter (surface roughness $= 2.0 \pm 0.2$ nm) at temperatures of 77 and 298 K.

roughness scattering on electrons, especially in miniaturized and surface disordered NWs.

4. Conclusions

In summary, a systematic study of the surface roughness dependent electron mobility in InAs NWs is presented. The grown NWs show good crystallinity and well-controlled surface morphology without any surface coating or tapering. A detailed AFM study is performed to characterize the NW dimensions and surface conditions. By investigating the electrical characteristics of the fabricated NW FETs in the global back-gate configuration, the peak electron field-effect mobility is found to decrease with increasing surface roughness. Also, the low-temperature electrical measurements are then utilized to separate the influence of surface/interface traps as well as phonon scattering and further illustrate that the enhanced surface roughness scattering induces a degradation of the mobility in both miniaturized and surface disordered NWs.

Acknowledgments

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